

## Wet Soil Electronic Device-Transistor and its Application Circuit

<sup>1</sup>Shiv Prasad Kosta, <sup>2</sup>Yogesh M. Dubey, <sup>2</sup>Avinash Gour, <sup>1</sup>Yogesh P. Kosta and <sup>3</sup>Shakti Kosta

<sup>1</sup>Charotar Institute of Technology-Changa, Ta: Petlad, Dist: Anand, Gujarat, India

<sup>2</sup>Shri Ram Institute of Technology, Damoh Naka, Marhatal, Near I.T.I., Jabalpur (MP), India

<sup>3</sup>University of Santa Clara, California, USA

**Abstract:** For the first time a new concept of soil transistor configuration and its experimental realization from raw natural wet soil lump along with supporting experimental studies (Kosta) depicting measured soil device transistor performance data, parameter-wise (in tabular form and graphs) are presented. Speculative potential application scenario is envisaged.

**Key words:** Soil device, soil model, transistor characteristics, architecture configuration, linear resistor, switching behavior

### INTRODUCTION

During 2003-07 we predicted and experimentally realized and reported Kosta *et al.* (1985), Kosta *et al.* (2003), Kosta *et al.* (2004a, b) and Kosta *et al.* (2006) the following research study. Tree antenna (Kosta *et al.*, 1985), Cactus leaf amplifier and multi vibrator (Kosta *et al.*, 2003), Bio-mass (green leaf) active device diode (Kosta *et al.*, 2004a, b), or/and gates using 2 soil diodes (Kosta *et al.*, 2004b) and Natural soil electronic active device diode (Kosta *et al.*, 2006).

In this communication for the first time we report the soil transistor conceptualization and its realization in a natural raw wet soil lump of Goradu soil of Charotar region of Anand-Gujarat-INDIA. Till date to our knowledge no other research team has so far reported similar original research work i.e., the use of Nature's gift (sand, water, bio-mass) to make electronic/electrical circuits.

### THEORETICAL CONSIDERATION

**The electronic soil model character:** From first order of approximation a wet soil can be modeled as a solution/mixture of (minerals and their salts) particles dissolved in water. From the basic principles of chemistry this solution/mixture is ionic in nature. Therefore, the wet soil consists of positive and negative ions of mineral's/compound's molecules and atoms. These ions are relatively heavier (compared to conventional charged particles holes and electrons of semiconductor devices) and as such their velocity will be slower than velocity of holes/electrons.

In addition in the wet soil, chemical reaction like oxidation and reduction also occur and as such the evolution/absorption of electrons takes place in it.

Therefore, the wet soil contains the following charged particles, positive ions, negative ions and negative electrons which can be utilized, to realize the basic building blocks of any general electrical electronic circuits.

The utilized experimental Goradu soil (lump soil piece) was analyzed by Prof. Sundaram of Agricultural University of Anand-India. The soil has the following chemical characteristics.

Texture loamy (fine sand 75%) sand with silt (10%) and clay (7%)---pH 7.8%--- exchangeable cations---  $\text{Ca}^{+2}$  (5.6),  $\text{Mg}^{+2}$  (4.6)  $\text{Na} + (\text{0.19}) \text{K} + (\text{0.14})$ . Available  $\text{P}_2\text{O}_5$  (23.4 kg ha<sup>-1</sup>)  $\text{K}_2\text{O}$  (310 kg ha<sup>-1</sup>) S (22.80 mg kg<sup>-1</sup>) DTPA (mg kg<sup>-1</sup>) Zn (1.05) Fe (8.97) Cu (2.41) Mn (15.0).

As reported earlier the conventional passive electronic components (resistance R, capacitance C and electronic soil device diode) can be made from wet soil lump.

**Formation of a soil diode:** When 2 metallic wire probes A and B are inserted in the wet soil lump, with a separation "d" in the range of a millimeter or so a feeble potential difference (a few milli volt) is experimentally observed. When an external positive and negative voltages (forward and backward) are applied to these two probes (A and B) the device functions like a conventional diode (Fig. 1 and 2).

Under forward and backward bias conditions  $I_F/I_R$  currents vary from a few db to 15-20 db for a soil

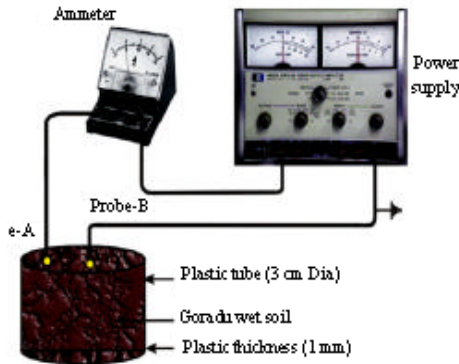


Fig. 1: Realization of a soil diode device

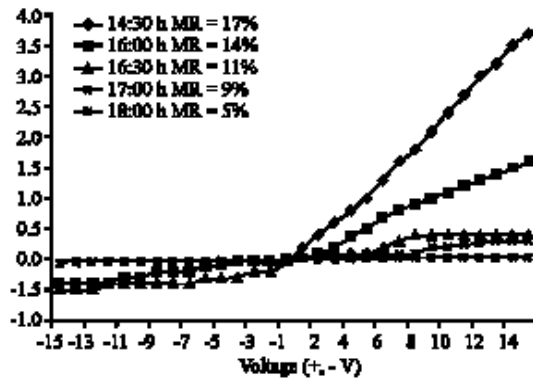


Fig. 2: Diode currents under forward and reverse bias condition

Moisture Ratio (MR) of the order of 20% (MR = weight of the water content divided by weight of dry soil). The results reported have been rigorously reproduced experimentally and found to be intact.

**First order approximate analysis (model wise) of electronic soil transistor:** Figure 3 depicts three terminal transistor device microstructure with architectural configuration including voltage-biasing scheme.

The transistor action can be visualized in the following 2 steps:

**Step 1: Building up the intuition:** The terminal 1 and 2 (Fig. 3) are basically separated along a straight line. When these 2 terminals are biased, basic V-I characteristics obviously result, however, their characteristic curves differ. This difference is attributed to the nature of the soil, MR ratio and the type of physical connections realized and largely to the heterogeneous nature of a structure of the soil itself. Also, as one can visualize/capture from the Fig. 3 of the microstructure the existence of wildly distributed ( $R$  and  $C$  elements) impedances

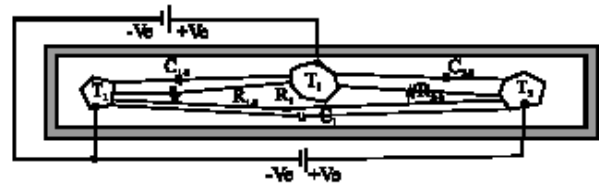


Fig. 3: Microstructure with architecture configuration of soil electronic transistor

(series between 2 realized paths/channels or of shunt types, forming other paths/channels realized or otherwise) consisting of resistance  $R$ , and capacitance  $C$ , (In the channel path and within the soil transistor, that purely depends upon its formation (skill and acumen of the fabricator) when probes (wires) are inserted). As said above, the value of  $R$ , and  $C$ , depends on the characteristics of soil moisture and these realized paths/channels etc., that make up the emitter, base and collector electrodes that eventually forms the characteristic of the paths/channels defining the nature of the soil device transistor. Extrapolating our thoughts a bit further in terms of measurable parameters, the path formed between terminal 1 and 2 has varying levels of conductivities  $\mu$  and  $\epsilon$  (That purely depends upon MR ratio and could be easily set). The conductivity could be either partially conducting or completely conducting or sometimes even non-conductive, we call this phenomenon as uneven distributed conductivities. Having built up this intuitive background helps us to crystallize upon the formation of a simple diode concept emerging from this physical configuration between terminal-1 and terminal-2. The characteristic of this (physically formed channel) is plotted in Fig. 4 and shown as line-2 (very much similar to a conventional semiconductor diode).

**Step 2:** When a third terminal (a few millimeters above;  $<2$  mm (max)) is introduced approximately perpendicular to the straight line joining terminal-1 and terminal-2, creates appropriate microstructure which modifies the conductivities between 1 and 2 (path/channel). In addition when DC potential is applied (biasing shown in Fig. 4) an alternation of fundamental V-I characteristics of the channel (between terminal 1 and 2) is created, that changes the slope of line-2 to line-3 as recorded in the plot of Fig. 4.

**Step 3:** When all the terminals are appropriately DC biased the new microstructure is created ( $R_1, C_1, R_2, C_2, R_3, C_3, R_4, C_4, R_5, C_5, R_6, C_6, R_7, C_7, R_8, C_8, R_9, C_9, R_{10}, C_{10}, R_{11}, C_{11}, R_{12}, C_{12}, R_{13}, C_{13}, R_{14}, C_{14}, R_{15}, C_{15}, R_{16}, C_{16}, R_{17}, C_{17}, R_{18}, C_{18}, R_{19}, C_{19}, R_{20}, C_{20}, R_{21}, C_{21}, R_{22}, C_{22}, R_{23}, C_{23}, R_{24}, C_{24}, R_{25}, C_{25}, R_{26}, C_{26}, R_{27}, C_{27}, R_{28}, C_{28}, R_{29}, C_{29}, R_{30}, C_{30}, R_{31}, C_{31}, R_{32}, C_{32}, R_{33}, C_{33}, R_{34}, C_{34}, R_{35}, C_{35}, R_{36}, C_{36}, R_{37}, C_{37}, R_{38}, C_{38}, R_{39}, C_{39}, R_{40}, C_{40}, R_{41}, C_{41}, R_{42}, C_{42}, R_{43}, C_{43}, R_{44}, C_{44}, R_{45}, C_{45}, R_{46}, C_{46}, R_{47}, C_{47}, R_{48}, C_{48}, R_{49}, C_{49}, R_{50}, C_{50}, R_{51}, C_{51}, R_{52}, C_{52}, R_{53}, C_{53}, R_{54}, C_{54}, R_{55}, C_{55}, R_{56}, C_{56}, R_{57}, C_{57}, R_{58}, C_{58}, R_{59}, C_{59}, R_{60}, C_{60}, R_{61}, C_{61}, R_{62}, C_{62}, R_{63}, C_{63}, R_{64}, C_{64}, R_{65}, C_{65}, R_{66}, C_{66}, R_{67}, C_{67}, R_{68}, C_{68}, R_{69}, C_{69}, R_{70}, C_{70}, R_{71}, C_{71}, R_{72}, C_{72}, R_{73}, C_{73}, R_{74}, C_{74}, R_{75}, C_{75}, R_{76}, C_{76}, R_{77}, C_{77}, R_{78}, C_{78}, R_{79}, C_{79}, R_{80}, C_{80}, R_{81}, C_{81}, R_{82}, C_{82}, R_{83}, C_{83}, R_{84}, C_{84}, R_{85}, C_{85}, R_{86}, C_{86}, R_{87}, C_{87}, R_{88}, C_{88}, R_{89}, C_{89}, R_{90}, C_{90}, R_{91}, C_{91}, R_{92}, C_{92}, R_{93}, C_{93}, R_{94}, C_{94}, R_{95}, C_{95}, R_{96}, C_{96}, R_{97}, C_{97}, R_{98}, C_{98}, R_{99}, C_{99}, R_{100}, C_{100}$ ). Upon application of varying AC input (from terminal 3) signal has the potential of changing the output characteristics (slope: channel conductivity and

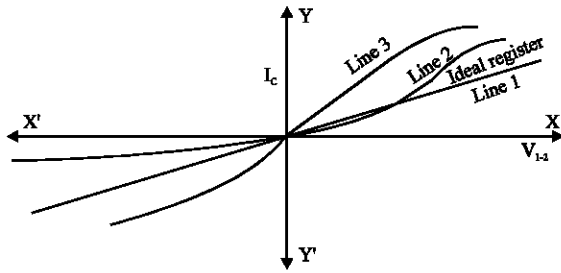


Fig. 4: Comparative response plot

resistance) as recorded (line-3) in Fig. 4. Line 1 depicts ideal characteristics of a junction (behaving as a simple linear register), Line 2 depicts practically recorded characteristics of the microstructure with terminal 3 unbiased and Line 3 depicts a slope due to biasing of terminal 3 confirming conductivity modulation.

Concluding that, we started with the creation of a simple Resistance channel ( $R_1$ ). That has a definite conductivity and a slope in the V-I characteristic curve depicting the value of resistance of the channel (between terminal-1 and terminal-2). When we proceed to add on a separate third terminal from the topside and appropriately bias it, this helped to change/modify the (modulate in case of AC signal) conductivity of the conducting path/channel (between terminal-1 and terminal-2) hence, the characteristic V-I slope, this is depicted as line-3 in Fig. 4. From the plots in Fig. 4, further as the power utilized in changing the conductivity (slope) is very less (10 times lesser in this case) compared to that required to bias it (terminal-1 and terminal-2), we can say that power gain is resulted and thus transistor action (through transfer of resistance). Thus we have established and we conclude that this is exactly the transfer of resistance vis-à-vis the depiction of transistor action.

Thus one can theoretically conceive soil electronic device transistor.

#### METHOD OF EXPERIMENTAL LABORATORY TRANSISTOR

**The laboratory (realization) wet soil transistor model:** To realize the soil transistor a small plastic bowl was filled with wet soil (around 20% Moisture Ratio) and three copper wire probes were inserted with appropriate spacing among them. The general physical soil transistor parameters were: bowl diameter = 25 mm, bowl height = 15 mm, probe wire diameter = (emitter = 1 mm, collector = 0.45 mm, base = 0.45 mm) and spacing among probe s = (between emitter and base around 1.5 mm, between base and collector around 3 mm) inserted depths d = 3, 2, 3 mm, respectively.

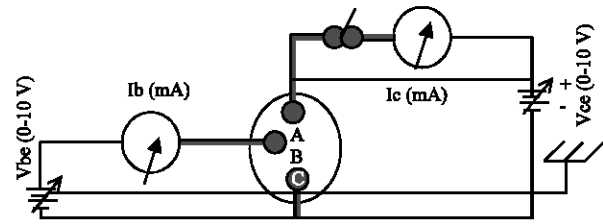


Fig. 5: Experimental measurement layout for input and output characteristics

Table 1: Recorded data for soil transistor input characteristics (Humidity = 30%, Room temperature = 26°C)

Vce open		Vce = 5 (V)	Vce = 10 (V)
Vbe (V)	Ib (mA)	Ib(mA)	Ib(mA)
0.5	0.01	0.00	0.00
0.6	0.03	0.02	0.01
0.7	0.06	0.04	0.04
0.8	0.08	0.07	0.07
0.9	0.11	0.10	0.09
1	0.13	0.12	0.11
2	0.44	0.43	0.41
3	0.73	0.79	0.73
4	1.03	1.02	1.01
5	1.32	1.33	1.32
6	1.63	1.63	1.63
7	1.95	1.92	1.91
8	2.23	2.22	2.21

**Experimental set-up for output characteristics measurement:** Schematic diagram of an experimental layout for soil transistor parameter measurement is depicted in Fig. 5.

#### RESULTS AND DISCUSSION

**The measured input characteristics:** Table 1 presents measured data and transistor input characteristics and Fig. 6 depict input characteristics of the experimental soil transistor table model. Here measurements were made for  $V_{be}$  and  $I_b$  keeping  $V_{ce}$  open circuited.

**The measured output characteristics:** Table 2 depict the output data characteristics of the wet soil lump device transistor. Here measurement were made to record collector current  $I_c$  for different value of  $V_{CE}$  keeping  $I_b$  constant.

#### SWITCHING BEHAVIOR OF SOIL TRANSISTOR/NOT LOGIC

The soil transistor was utilized to study the switching characteristics using the following experimental test circuit setup.

Table 2: Recorded data for soil transistor output characteristics (Humidity = 30%, Room temperature = 26°C)

Vce (V)	Ib = 10 uA			Ib = 20 uA			Ib = 40 uA			Ib = 50 uA		
	Ic (mA)	hfe	Vbe	Ic (mA)	hfe	Vbe	Ic (mA)	hfe	Vbe	Ic (mA)	hfe	Vbe
0	-0.03	-3	0.583	-0.02	-1.0	2.474	-0.05	-1.25	3.21	-0.04	-0.8	3.18
1	0.02	2	1.335	0.03	1.5	3.250	0.01	0.25	3.8	0.00	0.0	3.94
2	0.20	20	2.105	0.22	11.0	4.040	0.16	4.00	4.45	0.19	3.8	4.62
3	0.52	52	2.706	0.52	26.0	4.490	0.42	10.50	5.04	0.46	9.2	5.15
4	0.80	80	3.160	0.68	34.0	4.640	0.60	15.00	5.34	0.66	13.2	5.44
5	1.00	100	3.380	0.85	42.5	4.830	0.69	17.25	5.46	0.74	14.8	5.52
6	1.12	112	3.560	0.91	45.5	4.890	0.79	19.75	5.59	0.84	16.8	5.66
7	1.20	120	3.690	1.02	51.0	4.970	0.90	22.50	5.70	0.92	18.4	5.76
8	1.29	129	3.840	1.14	57.0	5.090	0.96	24.00	5.77	1.04	20.8	5.90
9	1.38	138	4.050	1.24	62.0	5.180	1.07	26.75	5.86	1.13	22.6	6.01
10	1.49	149	4.580	1.28	64.0	5.200	1.08	27.00	5.96	1.16	23.2	6.03
11	1.52	152	4.580	1.28	64.0	5.200	1.10	27.50	5.98	1.19	23.8	6.12
12	1.52	152	4.710	1.28	64.0	5.200	1.11	27.75	5.98	1.28	25.6	6.21
13	1.54	154	4.640	1.28	64.0	5.200	1.13	28.25	6.02	1.31	26.2	6.26

**Test setup apparatus:** Soil Transistor Device, power supplies (0-10 V) and (0-25 V), LED, Digital Multimeters for measurements of various currents and voltages (Fig. 7).

#### The circuit arrangement:

- Power supply  $V_{BE}$  is connected between base and emitter via two way switch so that in i) first condition  $V_{BE} = -V_{BE}$  and in ii) second condition  $V_{BE} = 0$
- Power supply between collector and emitter is ( $V_{CC}$ ) which is incorporated in circuit as shown
- LED is connected in series with collector along with a mili ampere meter to measure the current through collector circuit loop

#### Procedure:

- Switch was held in position A and measurement were made for  $V_{BE}$  and  $I_C$
- Switch was held at position B and measurements were repeated for  $V_{BE}$  and  $I_C$  (Table 3)

#### The discussion on switching behavior of the soil transistor:

- When switch K is held at A the  $V_{BE} = -V_{BE}$  and LED remains OFF therefore collector loop current  $I_C = 0$
- When switch is at B,  $V_{BE} = 0V$ , then LED remains ON and  $I_C$  flows through collector emitter circuit

From the above study, the switching behavior of soil transistor device is crystal clearly understood. Here one can easily understand that e when  $V_{BE}$  changes, current through collector emitter circuit  $I_C$  changes between zero and finite value.

**Explanation for NOT logic:** Theoretically in the NOT Logic when logic '1' input i.e. high voltage is applied at the base of common emitter configured transistor as switch, the current in collector circuit is high as transistor

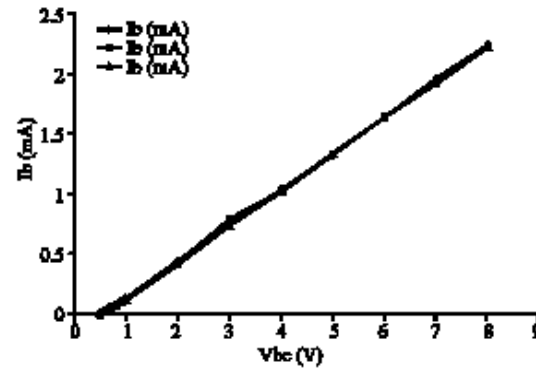


Fig. 6: Input characteristic of the transistor (soil MR = 20%)

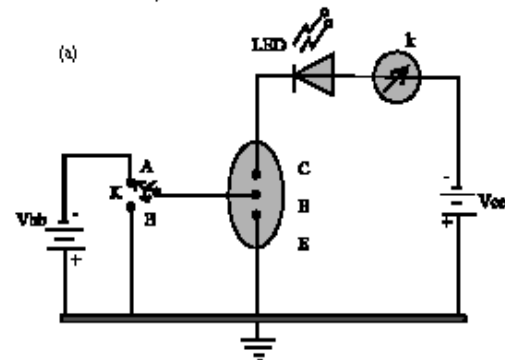


Fig. 7: Switching behaviour of soil transistor/NOT logic

Table 3: The observations

	$V_{BE}$ (V)	$V_{CC}$ (V)	$I_C$ (mA)	LED
1st observation	-6V	-6V	0	OFF
	0V	-6V	0.30	ON
2nd observation	-8V	-8V	0	OFF
	0V	-8V	0.45	ON

goes in saturation. Similarly when logic '0' input i.e., low voltage is applied at the base of the transistor the current in collector circuit is low or zero as transistor goes in cutoff region.

In the experiment performed using soil transistor setup similar results are observed. In the first observation when -6 volts is applied at the base of the soil transistor we did not get any current in the collector circuit and on the other hand when we applied 0 volts at the base of soil transistor we observed about 0.30 mA current flowing through the collector circuit and LED was turned ON. The collector voltage variation was not a pretty result but was observed to be changing between -5 and -4.61 volts.

### CONCLUSION

From in depth study of measured input and output characteristics of the performance data of the experimental wet-soil transistor, it is observed that the soil transistor concept and its realization (characteristics-wise) is in order. Speculatively, the feasibility of soil (micro-chip-set)

transistor seems to be clearly possible for technology development. Many technological problems will however, arise during technological feasibility studies which can be sorted out.

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