Journal of Engineering and Applied Sciences 8 (1): 15-20, 2013
ISSN: 1816-949X

Design of a 10-T Low Power Full Adder for VLSI Applications

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Abstract: Most of the Very Large Scale Integration (VLSI) applications such as digital signal processing, image processing, video processing and microcomputers extensively use arithmetic operations. The adder lies in the critical path of all the arithmetic operations so that it plays a crucial role in determining the overall system performance. Hence, low power dissipation, compact sized Integrated Circuit (IC) is highly required in modern digital applications. Recently, 10-Transistor Full Adder (10-T FA) becomes a good potential candidate for designing adder circuits because of reliable output and low power dissipation. This study presents the design and implementation of a low power 1-bit FA circuit. The design of the proposed full adder circuit is reducing power dissipation by optimizing the transistor size. The simulation results showed that the design required only 27×14.53 μm die area and dissipated as low as 0.1415 nW power. In comparison with previous studies, this proposed full adder demonstrates an advantage of low power dissipation and can be used at higher temperature with minimal power loss.

Key words: 10-T full adder, CMOS, VLSI application, XOR

INTRODUCTION

An explosive growth of integration of sophisticated multimedia-based applications into portable electronics devices are driving the design engineer to strive for higher speeds, long battery life and more reliable designs. Most of the VLSI applications, such as digital signal processing, image processing, video processing and microcomputers extensively use arithmetic operations (Akter *et al*., 2008a, b; Reaz *et al*., 2003, 2005, 2007a, b; Marufuzzaman *et al*., 2010; Sinha *et al*., 2011). Adder and subtractor circuit are widely used in electronic and communication systems, such as digital encoders, AM and FM modulation and neural networks (Reaz *et al*., 2006; Reaz and Wei, 2004; Mohd-Yasin *et al*., 2004; Mogaki *et al*., 2007). In most of these systems, the adder lies in the critical path that determines the overall system performance (Agrawal *et al*., 2010). In addition to its main task which is adding two binary numbers, it is the nucleus of many other useful operations such as subtraction, multiplication, division, addresses calculation, etc. (Leblebici and Kang, 1999; Rabaey, 1996). Consequently, building low power, high performance adder cells are of great interest and any modifications made to the full adder would affect the whole system. Thus by taking this fact into consideration, the design of a Full Adder (FA) that having low power results of great interest for the implementation of modern digital systems.

This study presents the design of low power 10-Transistors (10-T) full adder. The 10-T FA designed because this design produces reliable output and operates with low power dissipation. Simulation runs had conducted in different varying voltages and temperatures. At the earlier stages of designing a low power FA circuit, Wang *et al*. (2009) considered 8-Transistors (8-T) FA, however the output was not match the truth table of full adder even though the power is low. Then, FA with 11-Transistors (11-T) and more were designed but they produce high power. Consequently, the design of low power 10-T FA was proposed because it produces low power and the output was reliable. The function of FA is based on Eq. 1 and 2, three single bit inputs as A, B and C_{in} and it generates two outputs of single bit Sum and C_{out}, where:

$$Sum = (A \oplus B) \oplus C_{in} \quad (1)$$

$$C_{out} = A \bullet B + C_{in} (A \oplus B) \quad (2)$$

10-T 1-bit full adder architecture: Wang *et al*. (2009) and Sing *et al*. (2010) proposed 10-transistors full adder circuits. However, the design dissipates high power. The 8-transistors full adder circuit was also proposed in Wang *et al*. (2009) as well as Kumar *et al*. (2011) but were malfunction because when the circuit was redraw, the output was not satisfying the truth table of full adder. Another full adder circuit that was proposed by Hu and

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Wang (2011) has been redrawn to standardize the technology, temperature and voltage used as shown in Fig. 1.

According to the simulation output as shown in Fig. 2, the result was not reliable. When the input A = 1, B = 0 and C_{in} = 1 the result should be C_{out} = 1 and Sum = 0 but this circuit give the Sum = 1. Same goes to input A = B = C_{in} = 1, the output should be Sum = 1 and C_{out} = 1 but the result shows C_{out} = 1. Besides, the power dissipation is 0.2126 nW which is shown in Fig. 3.

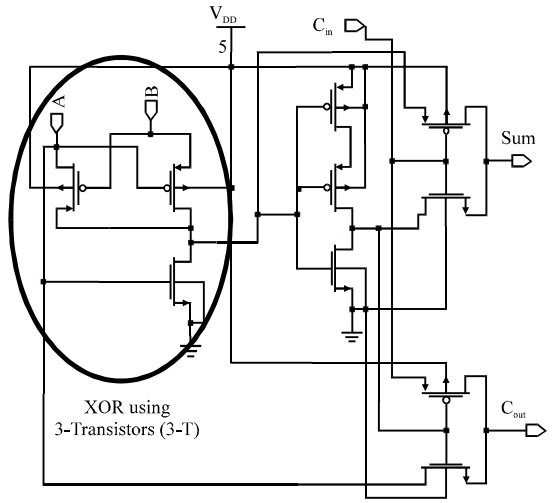


Fig. 1: 10-T full adder using 3-transistors for XOR

Proposed full adder architecture: One important requirement of full adder cells especially at low voltage is to provide enough driving power to the following circuits to ensure full signal swing to the stage of circuit which generate Sum and C_{out}. In this study, the proposed design with the combination of 4-transistors XOR, inverter and 2 multiplexers has been shown in Fig. 4. In this circuit, the gate lengths of all transistors have been taken as 0.18 μm. Width (W_n) of all NMOS transistors has been taken 1.0 μm and all of PMOS Width (Wp) has been taken as 2.0 μm. In XOR circuit as shown in Fig. 5 when A = B = 0 output is low because transistor P1 and and P2 are both on while both transistors N1 and N2 off. With input combination of A = 0 and B = 1 circuit shows high output as transistor P2 and N2 on, P1 and N2 are off. Same goes to input A = 1 and B = 0 high logic is passed to output because this time transistor P1 and N2 are in on condition. In case when A = B = 1, output shows low logic as transistor N1 and N2 discharge an output node rapidly.

Referring to Fig. 4, the second block is inverter. When the output of XOR connected to an inverter, it becomes an XNOR function. Sum is generated by C_{in}, XOR and XNOR while C_{out} is generated by A, XNOR and C_{in}. There are not signals generated internally that control the selection of the output multiplexers. Instead, the C_{in} input signal exhibiting a full swing and no extra delay is used to drive the multiplexers reducing so the overall

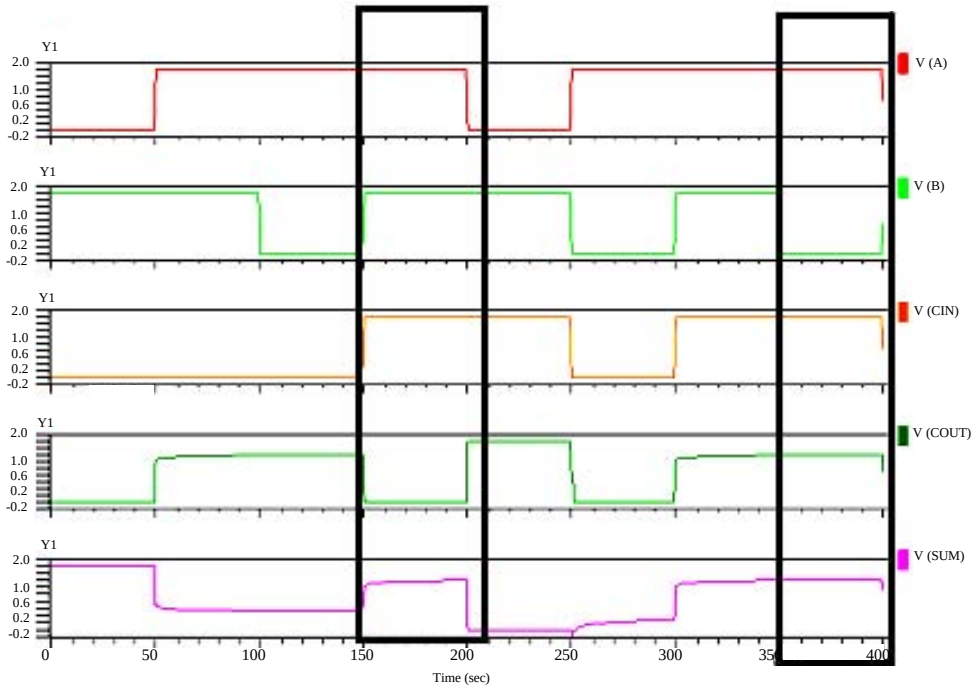
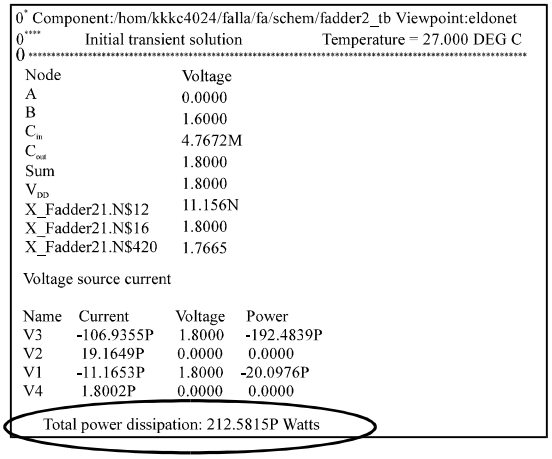


Fig. 2: Output waveform result of 10-T full adder using 3-transistors for XOR


0* Component:/hom/kkkc4024/falla/fa/schem/fadder2_tb Viewpoint:eldonet
0**** Initial transient solution Temperature = 27.000 DEG C
0 **********

Node	Voltage
A	0.0000
B	1.6000
C_{in}	4.7672M
C_{out}	1.8000
Sum	1.8000
V_{DD}	11.156N
X_Fadder21.N$12	1.8000
X_Fadder21.N$16	1.7665
X_Fadder21.N$420	

Voltage source current

Name	Current	Voltage	Power
V3	-106.9355P	1.8000	-192.4839P
V2	19.1649P	0.0000	0.0000
V1	-11.1653P	1.8000	-20.0976P
V4	1.8002P	0.0000	0.0000

Total power dissipation: 212.5815P Watts

Fig. 3: Power dissipation of 10-T full adder using 3-transistors for XOR

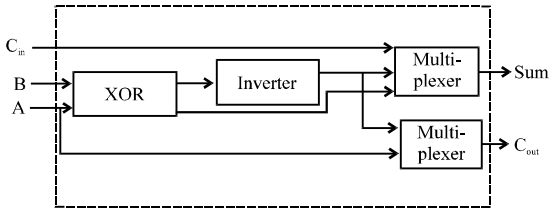


Fig. 4. Structure of the proposed full adder

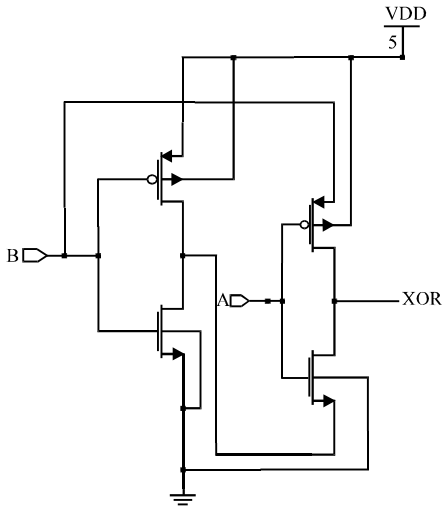


Fig. 5: 4-transistors XOR circuit

propagation delays (Aguirrre-Hernandez and Linares-Aranda, 2011). A single bit full adder using proposed 10-transistors has been implemented and shown in Fig. 6, simulations have been performed using Mentor Graphics Design Architecture IC (DA-IC) based on 0.18 μm CMOS technology with supply voltage of 1.8 V at 27°C.

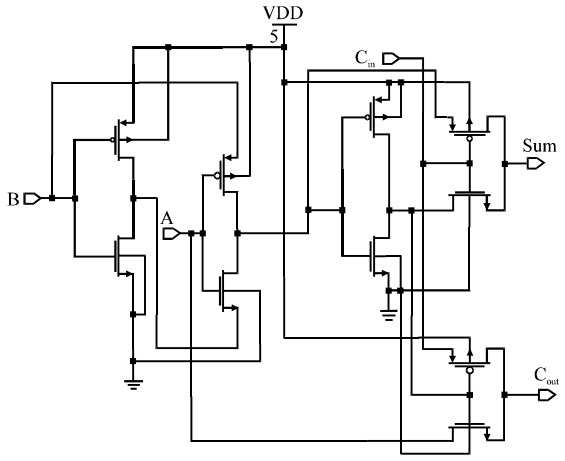


Fig. 6: Transistor level implementation of 1-bit 10-T FA circuit

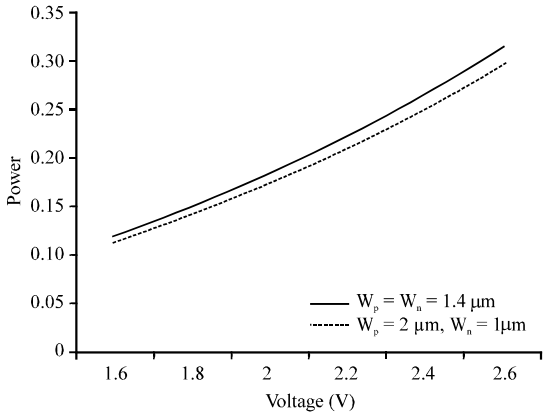


Fig. 7: Power dissipation of different width of PMOS and NMOS transistors

RESULTS AND DISCUSSION

Table 1 shows power dissipation with varying supply voltage 1.6-2.6 V for proposed full adder. Power dissipation varies from 0.1135-0.2961 nW with variations in supply voltage from 1.6-2.6 V (Fig. 7). Temperature varies from 7-67°C with variations in supply voltage from 1.6-2.6 V as shown in Fig. 8.

Power dissipation has been reduced due to the modification of width, 2.0 μm for PMOS (W_p) and 1.0 μm for NMOS (W_n). It has been observed from Table 1 that different width of CMOS will affect power dissipation.

The reasons are the relatively parasitic capacitances and the channel velocity saturation effect of submicron CMOS technologies (Rogenmoser and Kaeslin, 1997). By optimizing transistor sizes, the power dissipation

can be further reduced as shown in Fig. 7. Figure 8 shows power dissipation increases as the temperature rises.

Figure 9 shows the input and output waveform results for full adder. A wide range of simulation has been done from 1.6-2.6 V to see levels of output signal circuit which shows acceptable voltage levels are obtained from proposed circuit. As can be seen, the full adder has generated weak high and weak low in some input conditions. These occur because of threshold voltage. However, the output results satisfying the truth table of full adder as shown in Table 2.

Power dissipation for full adder in present research and earlier reported circuits are shown in Table 3. According to Table 3, even though proposed circuit has 10-transistors, it still shows low power dissipation as the proposed circuit is optimized the width of PMOS and NMOS.

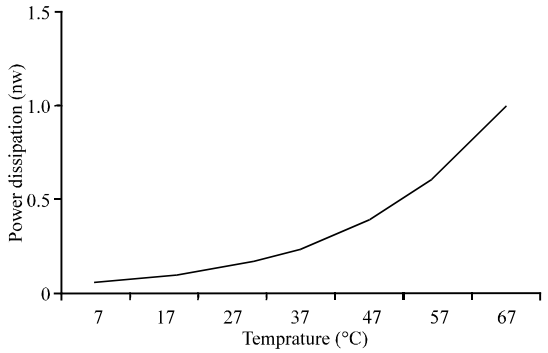


Fig. 8: Power dissipation of proposed full adder with temperature

Layout of the proposed circuit is shown in Fig. 10. The metal lines are placed horizontally at the top and bottom for the power supply (V_{DD}) and ground (V_{SS}). The layout area of the full adder is 27×14.53 μm. Based on the results, it is clear that the circuit not only reduce power but also occupy small die area.

Table 1: Power dissipation of proposed full adder with different width

	Power (nW)	
Voltage (V)	L = 0.18 μm $W_p = W_n = 1.4$ μm	L = 0.18 μm, W_p = 2 μm, W_n = 1 μm [proposed]
1.6	0.1199	0.1135
1.8	0.1496	0.1415
2.0	0.1834	0.1733
2.2	0.2217	0.2094
2.4	0.2649	0.2502
2.6	0.3135	0.2961

Table 2: Truth table of the proposed full adder

A	B	C_{in}	Sum	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table 3: Comparison between different types of full adder designs

References	No. of transistors	Power dissipation (nW)
Wang *et al.* (2009)	8	3504.0000
Singh *et al.* (2010)	10	69.5500
Hu and Wang (2011)	10	0.1595
Kumar *et al.* (2011)	8	0.3379
This research	10	0.1415

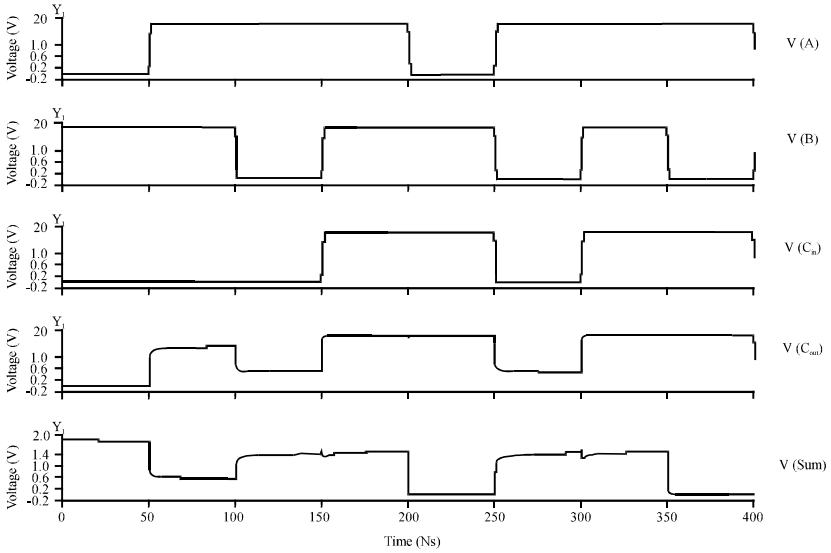


Fig. 9: Output waveforms of the proposed full adder

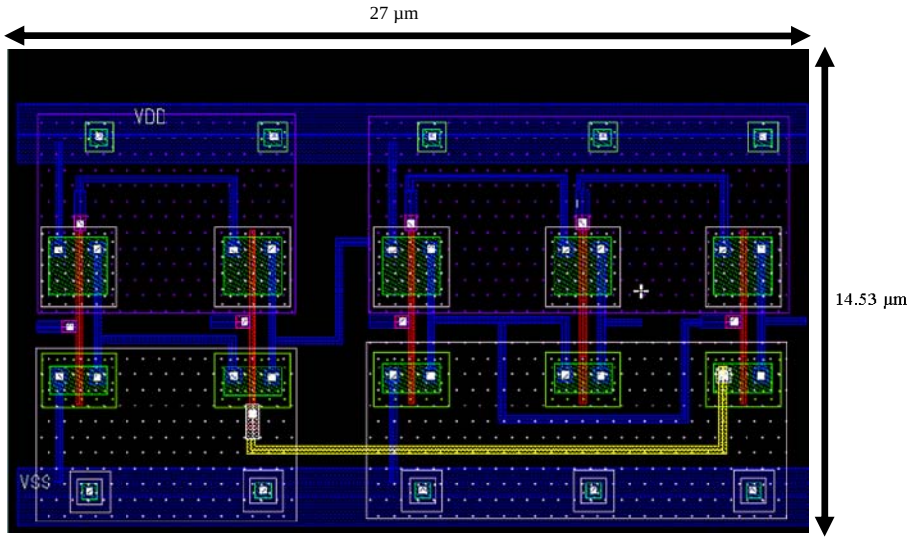


Fig. 10: Layout for proposed full adder

CONCLUSION

The proposed full adder cell consists of one XOR, one inverter and two multiplexers by optimizing size of all PMOS and NMOS transistors to achieve a reliable output result and low power dissipation compared to previous FA circuits. The simulation results showed that the proposed circuit dissipates only 0.1415 nW of power which is lowest among other researchers. Moreover, the layout design is done and found that the proposed design required only 392.31 μm^2 die area. From analysis of adder cells made by Shams *et al*. (2002), it was concluded that this adder cell can be used at higher temperature with minimal power loss.

REFERENCES

Agrawal, A.K., A. Mishra and R.K. Nagaria, 2010. Proposing a novel low-power high-speed mixed GDI full adder topology. Proceeding of the International Conference on Power, Control and Embedded Systems, November 29- December 1, 2010, Allahabad, India, pp: 1-6.

Aguirrre-Hernandez, M. and M. Linares-Aranda, 2011. CMOS Full-adders for energy-efficient arithmetic applications. Trans. Very Large Scale Integration Syst., 19: 718-721.

Akter, M., M.B.I. Reaz, F. Mohd-Yasin and F. Choong, 2008a. A modified-set partitioning in hierarchical trees algorithm for real-time image compression. J. Commun. Technol. Elect., 53: 642-650.

Akter, M., M.B.I. Reaz, F. Mohd-Yasin and F. Choong, 2008b. Hardware implementations of an image compressor for mobile communications. J. Commun. Technol. Elect., 53: 899-910.

Hu, J. and J. Wang, 2011. Low power design of a full adder standard cell. Proceedings of the 54th IEEE International Symposium on Circuits and Systems, August 7-10, 2011, Ningbo, China, pp:1-4.

Kumar, M., S.K. Arya and S. Pandey, 2011. Single bit full adder design using 8 transistors with novel 3 transistors XNOR gate. Int. J. VLSI Des. Commun. Syst., 2: 47-59.

Leblebici, Y. and S.M. Kang, 1999. CMOS Digital Integrated Circuits. 2nd Edn., McGraw Hill, Singapore.

Marufuzzaman, M., M.B.I. Reaz and M.A.M. Ali, 2010. FPGA Implementation of an intelligent current dq PI controller for FOC PMSM drives. Proceedings of the International Conference on Computer Applications and Industrial Electronics, December, 5-7, 2010, Kuala Lumpur, Malaysia, pp: 600-603.

Mogaki, S., M. Kamada, T. Yonekura, S. Okamoto, Y. Ohtaki and M.B.I. Reaz, 2007. Time-stamp service makes real-time gaming cheat-free. Proceedings of the 6th Annual Workshop on Network and Systems Support for Games: Netgames 2007, September 19-20, Melbourne, Australia, pp: 135-138.

Mohd-Yasin, F., A.L. Tan and M.I. Reaz, 2004. The FPGA prototyping of iris recognition for biometric identification employing neural network. Proceedings of the 16th International Conference on Microelectronics, December 6-8, 2004, Tunis, Tunesia, pp: 458-461.

Rabaey, J., 1996. Digital Integrated Circuits: A Design Perspective. Prentice Hall, Englewood Cliffs, NJ.

Reaz, M.B.I. and L.S. Wei, 2004. Adaptive linear neural network filter for fetal ECG extraction. Proceedings of the International Conference on Intelligent Sensing and Information Processing, January 4-7, 2004, Chennai, India, pp: 321-324.

Reaz, M.B.I., F. Mohd-Yasin, S.L. Tan, H.Y. Tan and M.I. Ibrahimy, 2005. Partial encryption of compressed images employing FPGA. Proceedings of the IEEE International Symposium on Circuits and Systems, May 23-26, 2005, Kobe, Japan, pp: 2385-2388.

Reaz, M.B.I., F. Choong and F. Mohd-Yasin, 2006. VHDL modeling for classification of power quality disturbance employing wavelet transform, artificial neural network and fuzzy logic. Simulation, 82: 867-888.

Reaz, M.B.I., F. Choong, M.S. Sulaiman and F. Mohd-Yasin, 2007a. Prototyping of wavelet transform, artificial neural network and fuzzy logic for power quality disturbance classifier. Elect. Power Compon Syst., 35: 1-17.

Reaz, M.B.I., M.I. Ibrahimy, F. Mohd-Yasin, C.S. Wei and M. Kamada, 2007b. Single core hardware module to implement encryption in TECB mode. Informacije MIDEM J. Microelect. Elect. Compon. Mater., 37: 165-171.

Reaz, M.B.I., M.T. Islam, M.S. Sulaiman, M.A.M. Ali, H. Sarwar and S. Rafique, 2003. FPGA realization of multipurpose FIR filter. Proceedings of the Parallel and Distributed Computing, Applications and Technologies, August 27-29, 2003, Chengdu, pp: 912-915.

Rogenmoser, R. and H. Kaeslin, 1997. The impact of transistor sizing on power efficiency in submicron CMOS circuits. IEEE J. Solid-State Circuits, 32: 1142-1145.

Shams, A.M., T.K. Darwish and M.A. Bayoumi, 2002. Performance analysis of low-power 1-bit CMOS full adder cells. IEEE Trans. Very Large Scale Integr. Syst., 10: 20-29.

Singh, A.K., C.M.R. Prabhu, K.M. Almadhagi, S.F. Farea and K. Shaban, 2010. A proposed 10-T full adder cell for low power consumption. Proceedings of the International Conference on Electrical Engineering/ Electronics Computer Telecommunications and Information Technology, May 19-21, 2010, Keroh, Malaysia, pp: 389-391.

Sinha, D., T. Sharma, K.G. Sharma and B.P. Singh, 2011. Design and analysis of low power 1-bit full adder cell. Proceedings of the 3rd International Conference on Electronics Computer Technology, April 8-10, 2011, Lakshmangarh, India, pp: 303-305.

Wang, D., M. Yang, W. Cheng, X. Guan, Z. Zhu and Y. Yang, 2009. Novel low power full adder cells in 180nm CMOS technology. Proceedings of 4th IEEE Conference on Industrial Electronics and Applications, May 25-27, 2009, Xian, China, pp: 430-433.