Journal of Engineering and Applied Sciences 11 (10): 2161-2175, 2016
ISSN: 1816-949X

Solar Powered Multi-Module Cascaded Multi Level Inverter Drive for Permanent Magnet Synchronous Motor

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Abstract: The Permanent Magnet Synchronous Motors (PMSM) are replacing the asynchronous motors in traction applications. The efficiency of the motor depends on the efficiency of the inverter drive circuit. Several Multi-Level Inverters (MLI) are discussed. To improve the performance of PMSM, Multi-Module Multi Level Cascaded Inverter (MMCMLI) is designed with phase disposition modulation algorithm. The MMCMLI is powered by solar energy with maximum point tracking. The entire design is simulated in Matlab/Simulink. The incremental conductance maximum power point tracking control is discussed in detail. The design of 3, 5, 7 and 9 level MMCMLI is shown with the phase disposition modulation algorithm. Finally the designed converters are combined with the battery bank and PMSM. The performance of PMSM with 3, 5, 7 and 9 level inverter is discussed. Also the phase current and speed variation of PMSM at different operating frequencies below and above the rated frequencies is analyzed. The voltage and current THD analysis of different level of the MMCMLI shows that the voltage harmonics decreases with increase in the level whereas the current harmonics stays at an average level which increases the stability of motor operation at frequencies below the rated frequency.

Key words: Permanent magnet synchronous motor, incremental conductance, multi-module multi-level inverter, phase disposition, diode clamped multilevel inverter, flying capacitor multilevel inverter

INTRODUCTION

In traction drive applications, Permanent Magnet Synchronous Motors (PMSM) are now replacing asynchronous motors (Krishna, 2010). In long distance rail transport and short distance tram operations, energy efficiency is an important factor (Demmelmayr *et al*., 2011). The PMSM are high power density, efficient and capable operating at wide speed ranges compared to induction motors (Soleimani and Vahedi, 2012). Due to this fact the research in the field of traction drive application using PMSM is consistently improving. The efficient operation of PMSM in traction application is based on the efficiency of the inverters used. Commonly, Multi-Level Inverters (MLI) are used in traction applications to drive PMSM.

The MLIs are power electronic devices that are built to synthesize a desired ac voltage from several levels of dc voltages. Due to the increased power demand, the MLIs are finding increased attention in industries as one of the preferred choices of electronic power conversion for high-power applications (Rodriguez *et al*., 2002). In the beginning, the term multilevel began with the three level converters. Later, several multilevel converter topologies have been developed (Vidhayathil, 1995). Multilevel inverters include an array of power semiconductors and capacitor voltage sources, the output of which generate voltages with stepped waveforms (Lai and Feng, 1996). The commutation of the switches permits the addition of the capacitor voltages to reach high voltages at the output. The increase in the number of levels, decreases the harmonic distortion of the output voltage. However, a higher number of levels increases the control complexity and introduces voltage imbalances (McGrath and Holmes, 2002). To reduce the voltage imbalance, various topologies for MLIs have been proposed but only two of them have received considerable interest for high-power inverter systems manufacturers (Vidhayathil, 1995). These inverter topologies for MLIs are diode-clamped MLI (DCMLI) and Flying Capacitor MLI (FCMLI) (Rodriguez *et al*., 2002) (Vidhayathil, 1995). Other MLI structures have also been proposed. However, most of them are either hybrid combinations or modifications of the above mentioned MLIs (Kedareswari, 2013).

In diode-clamped MLI, diodes are used as clamping devices in each phase of the inverter. Different voltages are obtained from the dc input by the use of capacitors in series. These different voltages are supplied to the output using properly controlled static switches such that a multilevel staircase sinusoidal voltage waveform is produced (Kedareswari, 2013). The advantage of this method is that it eliminates the need of output filters if the number of levels is significantly high. Another

advantages of this method is that the switching frequency can be as low as the fundamental frequency (low frequencies result in lower the stress on the switches) (Yuan and Barbi, 2000). The drawbacks of this method includes the indirect clamping of the switching devices, turn-on snubbing for the inner dc rails, multiple blocking voltage of the clamping devices, difficulties in the control of power flow and the increase in the number of diodes as the number of levels increases (Islam *et al*., 2013).

The FCMLI has been proposed to eliminate few of the drawbacks of DCMLI. The structure of this inverter is similar to that of the DCMLI except that the clamping diodes are replaced by capacitors. Similar to DCMLI, the dc side capacitors divide the input dc voltage into different voltage increments. These voltage increments are used to formulate the steps in the output voltage waveform. The advantages of FCMLI include the availability of phase redundancies for balancing the voltage levels of the capacitors. Also, the presence of large number of capacitors enables the inverter to ride through short duration outages and deep voltage sags. The major drawbacks of FCMLI is the complexity in the control algorithm to track the voltage levels of all capacitors and the cost of the large number capacitors used (Andreas, 2011).

The performance of flying capacitor, neutral point clamped and cascaded H-bridge 5-level inverter using carrier based sinusoidal pulse width modulation is designed and compared (Abdelaziz *et al*., 2013). This study concludes that the carrier based H-bridge 5-level inverter is best suited for PV system input. It can be seen that the voltage THD of all the three topologies discussed are high due to the chosen modulation technique.

Many researches has been conducted on MLI and few researches which contributes significantly to the improvement of the design is discussed here. A multi-level inverter with reduced number of switches and selective harmonic elimination method is designed (Khounjahan *et al*., 2015). In this study, the 9-level inverter is achieved with reduced number of switches whereas the output voltage is heavily affected by the leakage inductance of the transformer.

A 5-level (Kavitha *et al*., 2012) and 11-level (Aditya 2014) cascaded inverter with different combination of number of switches and sources using different modulation techniques is discussed. In both the discussions, the voltage THDs are maintained almost the same for all the modulation methods. A 5-level three phase cascaded hybrid multi level inverter using pulse width modulation techniques is designed by (Thongprasri, 2011) using FPGA controller. The pulse width modulation technique reduces the current harmonics but not the voltage harmonics. A 7-level inverter using 5 switches is simulated and the design is tested with different modulation techniques (Umashankar *et al*., 2013). This design proves to be efficient is reducing the number of switches whereas the THD are not reduced considerably. A 7-level inverter with single DC source is introduced for electric vehicle propulsion. This method uses two inverters; main and auxillary. Though this method eliminates the need of hysteresis comparators and look up tables in the direct torque control method, it increases the complexity of the control circuit.

The cascaded multi-level inverter at 11-level (Bhaskar *et al*., 2014) and 5-level using pulse width modulation techniques are discussed. These papers aims at reducing the number of switches and DC sources whereas with the proposed pulse width modulation methods the voltage THDs are not reduced to low level.

A multi carrier phase shift pulse width modulation technique is proposed for a transistor clamped H-bridge inverter (Lakshmipriya *et al*., 2015). Though this method decreases the THD in the output voltage at 13 level, the power quality and losses are compensated.

The requirement of multiple input sources are one of the widely discussed area in cascaded multi-level inverter research. A method to use single DC source with capacitors to produce a nearly sinusoidal voltage output is proposed. This method eliminates the need of multiple DC sources at the input but it compromises the quality of the output voltage and current.

Various topologies has been discussed to effectively utilize the renewable energy sources at the input. A 11-level modular multilevel inverter to connect the wind turbine to the grid is proposed. The control strategy used effectively monitors the active and reactive power. Also, the power factor of the local power line is maintained constant irrespective of the variation in the power from wind turbine.

To improve the performance of the MLI and decrease the complexity in the control algorithm, many artificial intelligence techniques has been proposed. The step modulation method is proposed for 11-level multi carrier inverter. Fuzzy logic controller is introduced to replace the I controller at the output of the inverter. The reduction in current and voltage harmonics is seen in this indirect method.

A 15-level cascaded inverter using bee alogirthm is also proposed (Jesline and Ramraj, 2014). It can be seen that the proposed algorithm decreases the complexity of the switching algorithm with reduced THD.

The performance of flying capacitor, neutral point clamped and cascaded H-bridge 5-level inverter using carrier based sinusoidal pulse width modulation is

designed and compared (Abdelaziz *et al*., 2013). This study concludes that the carrier based H-bridge 5-level inverter is best suited for PV system input. It can be seen that the voltage THD of all the three topologies discussed are high due to the chosen modulation technique.

The efficiency of the inverter plays a major role in increasing the efficiency of PMSM in traction applications. In this study, multi-module cascaded multi-level inverter with separate dc sources is implemented as a drive circuit to operate PMSM at different frequencies efficiently. To reduce harmonics and to increase the performance of PMSM phase in disposition modulation method is used. Also the Maximum Power Point Tracking (MPPT) of the solar panel using Incremental Conductance algorithm is discussed in detail. This paper is proceeded in three levels. At the first level of research, the advantages of using incremental conductance MPPT control compared to the other methods and the control algorithm is discussed. At the second level,different level of multi-module cascaded multi-level inverter is tested. At the third level the closed loop system is designed to drive PMSM at frequencies using different levels of multi-module cascaded multi-level inverter. The proposed design is simulated in matlab/simulink.

MATERIALS AND METHODS

Design of solar panel, MPPT and boost converter: This design includes the use of solar panel with maximum power point tracking boost converter to act as the power source for multi-module cascaded multi-level inverter to drive PMSM at different operating frequencies. The generalized block diagram of the design is shown in Fig. 1.

There are many MPPT methods implemented such as Perturb and Observe (P and O), Incremental Conductance (IC), Hill Climbing and Parasitic Capacitance method. Of these the commonly used methods are P and O and IC algorithms. The major drawback of P and O algorithm is that it never reaches the maximum power point but oscillates around the point of maximum power (Latif and Hussain, 2014) (Meng *et al*., 2014; Harish and Prasad, 2013). Though IC method is much more complex than P and O algorithm, due its accuracy in tracking maximum power point, IC method is chosen for driving boost converter. The IC algorithm is derived by differentiating the PV output power with respect to voltage and equating it to zero. In this algorithm the controller continuously measures the parameters of the PV panel and checks whether the resultant derivative is equal to zero or not. If it is not zero, then the controller will decide in which direction a perturbation mustt occur in order to bring it to the maximum power point. The algorithm of IC is explained in the flow chart shown in Fig. 1. The solar panel and MPPT algorithms are tested using Matlab. The Tenesol TO505 solar panel is modelled using basic PV array equations and tested at a constant temperature of 22°C. The P-V characteristic of the panel at 22°C under varying irradiance level is shown in Fig. 2.

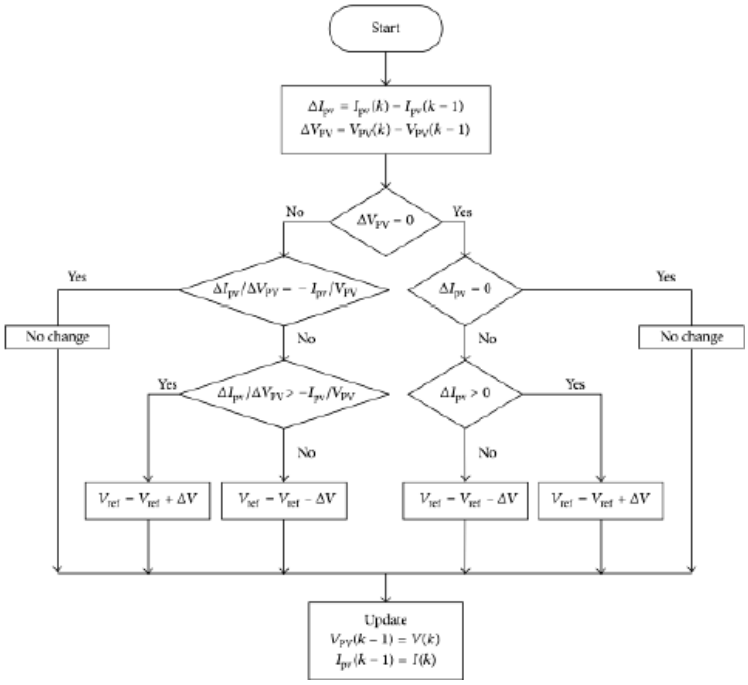

Fig. 1: IC algorithm for boost converter

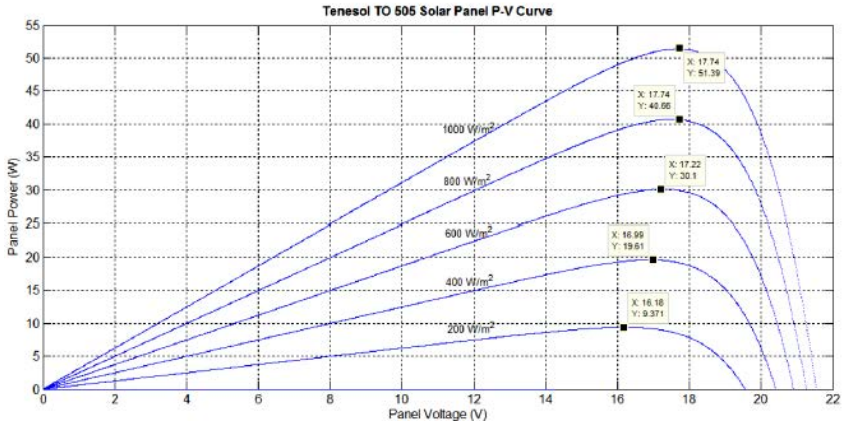

Fig. 2: Solar panel at 22°C under varying irradiance level

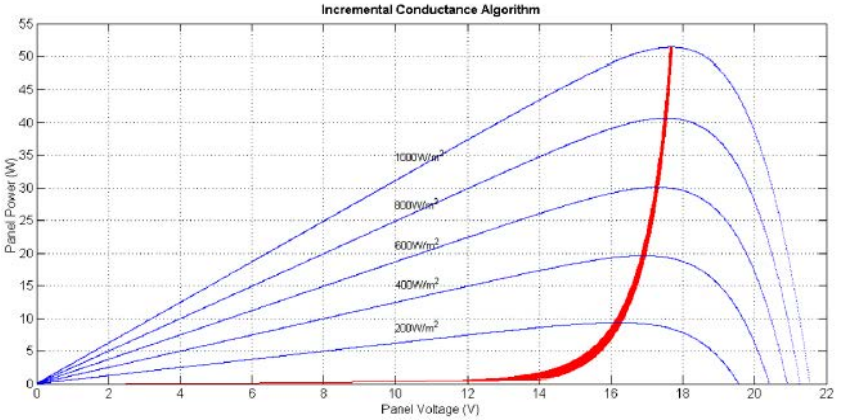

Fig. 3: IC algorithm on Tenesol TO 505 panel

The MPPT algorithm is applied to determine the maximum power points for the entire range of expected irradiation levels at 22°C. The incremental conductance algorithm test on solar panel is shown in Fig. 3.

It can be seen from Fig. 4 that the IC algorithm is tracking the power point for any increase in the irradiance level. Also in IC method there is a provision to stay at a certain level once maximum power point is tracked. Using the data collected from the modelled PV panel, the inductor and capacitor of the boost converter is calculated. The closed loop boost converter is applied with IC algorithm steps to ensure that the duty cycle varies according to the variation in the input to maintain constant output required for the inverter.

Design of multi-module cascaded multi-level inverter: The multi-module cascaded inverter consists of single phase full bridge inverters that are connected in series according to the number of levels required at the output voltage. The general function of this inverter is to synthesize the desired voltage from several DC source voltages which may be obtained from batteries, fuel cells or renewable energy sources. The Multi-module Cascaded Multi-level Inverter (MMCMLI) has the advantage of using fewer components than the other topologies, the major disadvantages of the MMCMLI is the requirement of separate dc sources for each H-bridge (Manjirekar and Lipo, 1994) and complex control circuit when the separate dc sources are merged as a single source. Figure 4 shows a single-phase structure of the cascaded inverter with Separated DC source (SDCs). Each single phase full bridge (or H-bridge as it traditionally referred) inverter is connected with separate DC sources. The DC source can be a battery source or any renewable energy source. Each inverter level can generate three different voltage outputs, by connecting the dc source to the ac output through different combinations of the four switches S_1, S_2, S_3 and S_4. To obtain $+V_{dc}$, switch S_1 and S_4 are turned on. To obtain $-V_{dc}$, switch S_2 and S_3 are turned on. Turning on S_1 and S_2 or S_3 and S_4 will produce 0V. The ac output of each of the different level full-bridge inverters are connected in series such that the synthesized

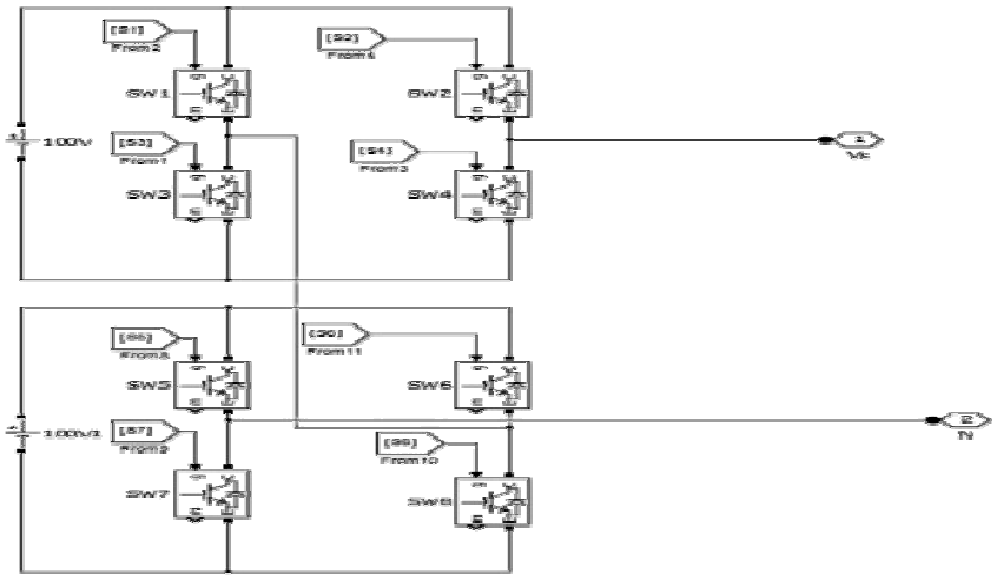

Fig. 4: Single phase structure of cascaded inverter

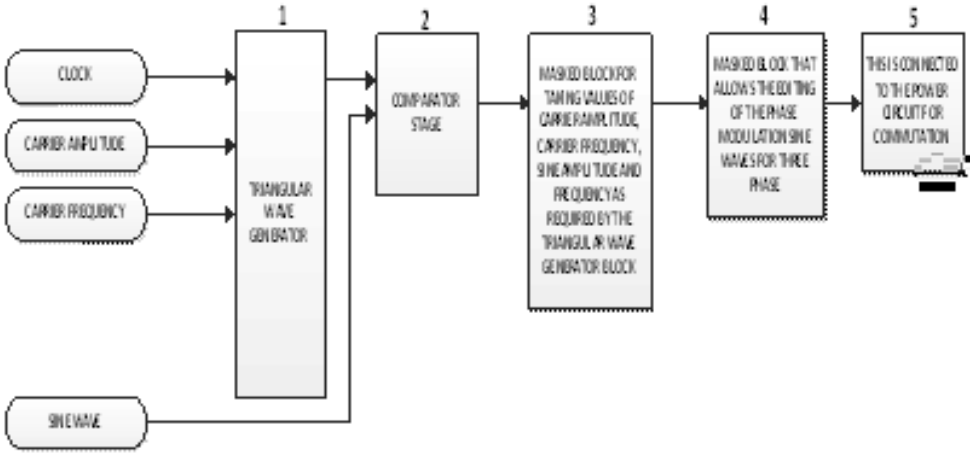

Fig. 5: Simulink model of Switching circuit

voltage waveform is the sum of the inverter outputs. The number of output phase voltage levels in a cascade-inverter is determined by:

$$m = 2s+1$$

Where:
s = The number of DC source
m = Represents the number of level

Mmcmli modulation method: Multilevel inverters highly rely on the control signals produced by the control circuitry. The control signals are based on the type of modulation strategy chosen for particular application. In multi-level inverters, the pulse width modulation methods are classified into multi carrier pulse width modulation and space vector pulse width modulation methods. The multi carrier pulse width modulation strategy is further classified into several modulation methods discussed in the literature study based on the type of carrier wave. In this research phase disposition method is employed to reduce the output harmonics and improve the starting characteristics of PMSM.

The block diagram of generation of triggering signal is shown in Fig. 5. The design stages shown in Fig. 2 are design and simulation of the triangular wave generator, comparator stage, design and simulation of the system with block 3 and 4.

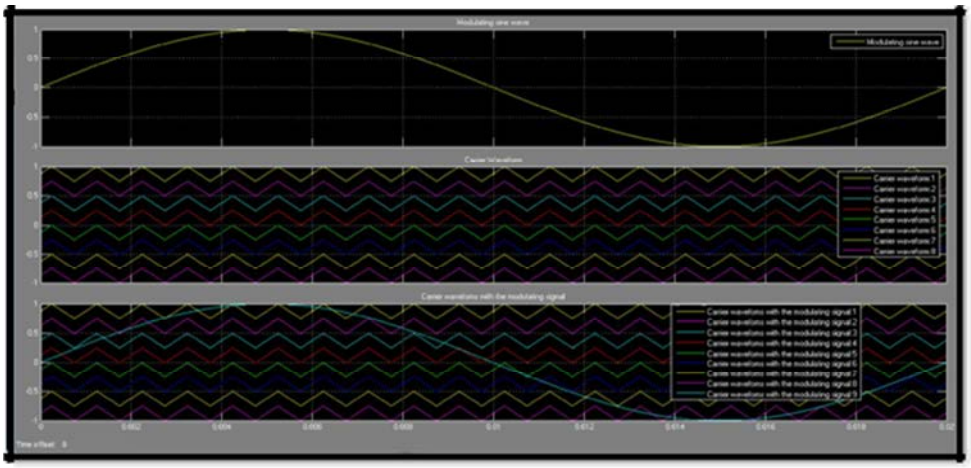

Fig. 6: Input signal to the comparator

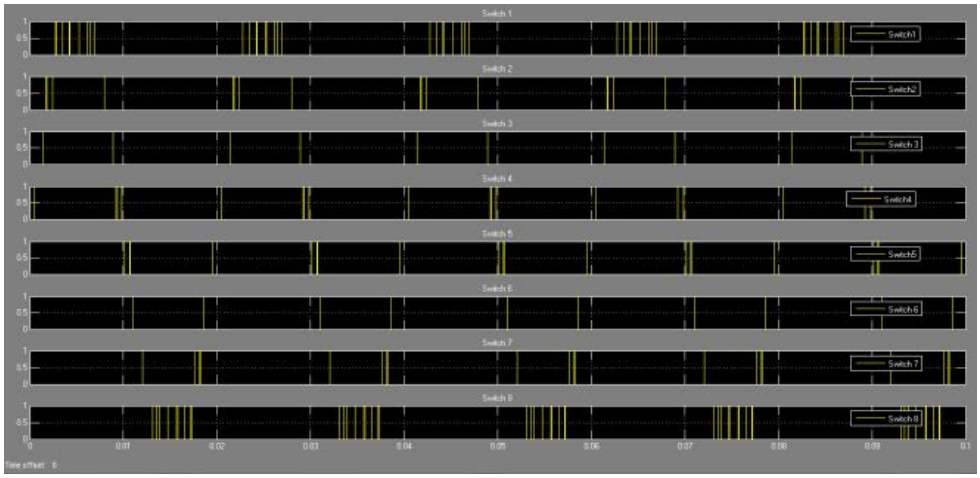

Fig. 7: Output signal from the comparator

The switching signals produced in block 2 are supplied to the triggering terminals of the IGBTs in the power circuit. The signals are further complemented to provide switching for the rest of the switches in the power circuit.

Block 1 generates triangular waveforms using phase disposition modulation mode. The characteristic of this method is that the carrier waveforms having similar frequency and amplitude but different dc offset to adjoining bands. The phase disposition modulation method is chosen because harmonic content on line-line output is very less compared to Alternate Phase Disposition (APD) and Sinusoidal Pulse Width Modulation (SPWM) methods. Also in phase disposition method, the harmonic energy is directly injected into a common mode carrier component which allows the harmonics to cancel in the line-line output voltage. Figure 6 shows the generated modulating sine signal (first axis), carrier signals (middle axis) and both carrier and modulating signals on the same system of axis (last axis). The waveforms are generated at an amplitude modulation index of 0.25 and carrier frequency of 10 kHz which makes the inverter to operate in the linear mode.

The comparator stage is shown in block 2 in Fig. 7. In this block, carrier signals are compared with the with the modulation sine wave. If carrier signal is less than the modulating signal, logic high is produced at the comparator output and a logic low signal is produced if the carrier signal is lower than the modulating signal. This comparison is performed for each of the carrier signals with the modulating sine wave. The eight square wave signals are produced from the comparator signals using based on the sinusoidal pulse width modulation. The output of the comparator block is shown in Fig. 7. The switching signal generated for each IGBT is shown in Fig. 8.

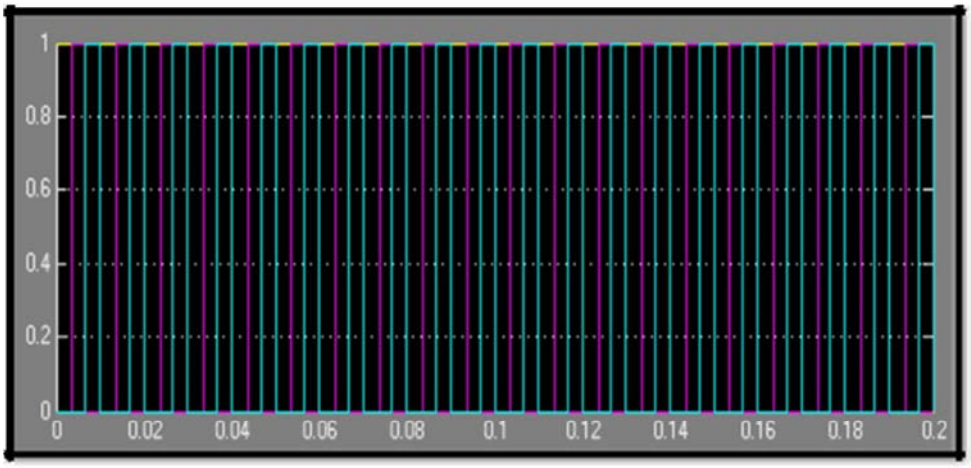

Fig. 8: Switching signal for IGBT

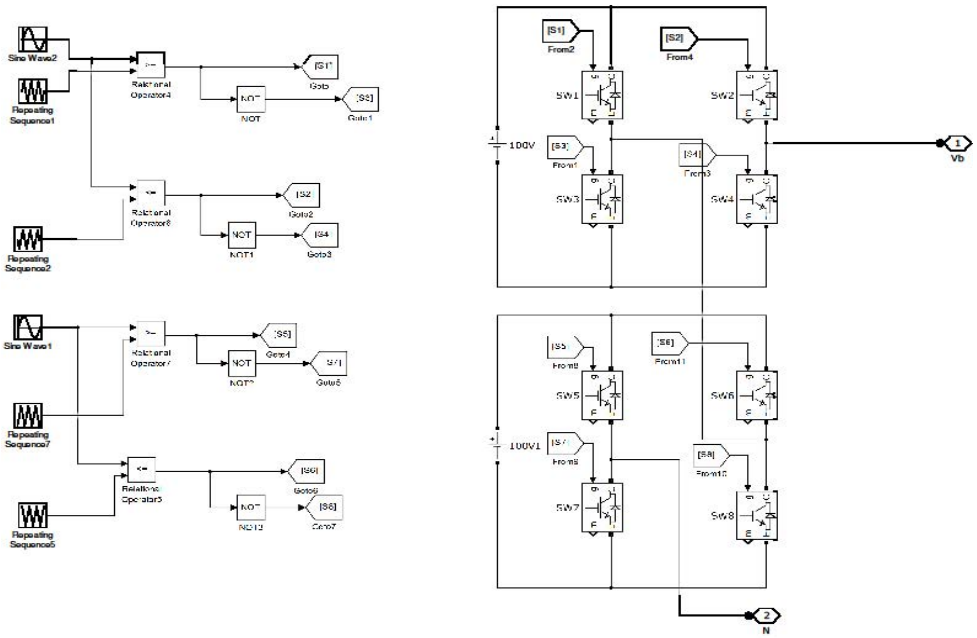

Fig. 9: Simulink model of MMCMLI

MMCMLI power circuit: The power circuit consists of the input battery pack, the switching devices (diodes and IGBTs) and the PMSM. The circuit diagram of the power circuit is shown in Fig. 9. In high power applications such as electric vehicles, the IGBTs are highly preferred as a switching device because of its higher power handling capabilities.

The switching table of the triggering signals is shown in Table 1. The switching signals are required by the power circuit switches for half cycle. The design is based on the 1MBI1200U4C-120 IGBT due to its on-voltage drop of 1.93 V and a zero-gate collector current (which is similar to the leakage current) of 1 mA. From Table 1, it can be seen that each half cycle requires that 4 switches be on and 4 be off. For the on switches, the current that flows

Table 1: Switching table of MMCMLI

Variables	Values							
V_{ao}	1	2	3	4	1'	2'	3'	4'
V_{dc}	1	1	1	1	0	0	0	0
(¾)V_{dc}	0	1	1	1	1	0	0	0
Vdc/2	0	0	1	1	1	1	0	0
Vdc/4	0	0	0	1	1	1	1	0
0	0	0	0	0	1	1	1	1

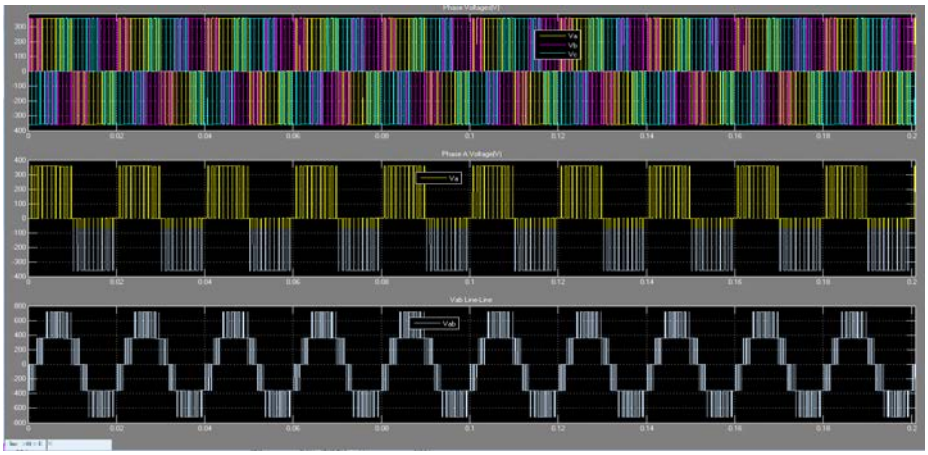

Fig. 10: Three level MMCMLI output voltages

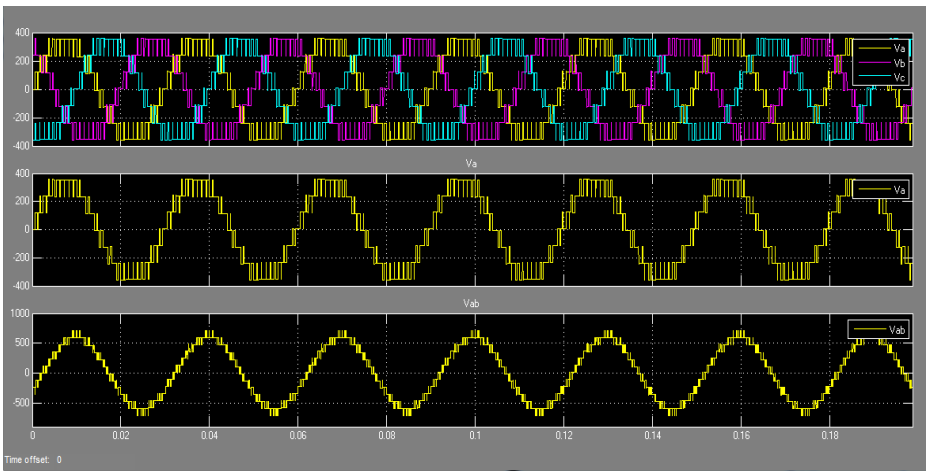

Fig. 11: Five level MMCMLI output voltages

through them is equal to the output current of the inverter and the voltage across them is 1.93. For the off switches, the current through them is equal to the leakage current (1 mA) and the voltage across them is Vdc/4 which is equal to 90 v for the nine level MLI.

Design and analysis of MMCMLI with PMSM: The MMCMLI was also designed and simulated in Simulink. It consists of mainly the battery pack which is divided according to the number of levels in the inverter, the power circuit and the switching network. The inverter is loaded with the PMSM. The parameters of the synchronous machine are shown in Table 2. The output voltages of three, five, seven and nine level inverters are shown in Fig. 10-13.

Simulation results of MMCMLI: The system is basically an open loop system consisting of the battery, MLI and the machine. Power flows from the battery via the inverter to machine during motoring and it flows from the machine via the universal rectifier to the battery during braking. Fig. 14 shows the block diagram of the system.

Table 2: Parameters of PMSM

Parameter name	Parameter value
Stator resistance (R_s)	0.18 Ω
Armature Inductance (L_a	0.835 mH
Flux linkage established by magnets (Λ)	0.1429 At
Voltage constant (krpm)	51.8384
Torque constant	0.4287 N.m/A
Inertia constant (J)	0.0062 kg
Viscous damping constant (B)	0.3035 Nms
Number of poles (p)	2

In the generalized block diagram shown in Fig. 14, block 1 represents the input battery pack of 360 V. The capacity of the battery is 24 kWh but the for the optimum design the battery capacity must be as large as possible. The multilevel inverter stage is shown in block 2. The blocks 3, 4 and 6 operate as the controller for the system.

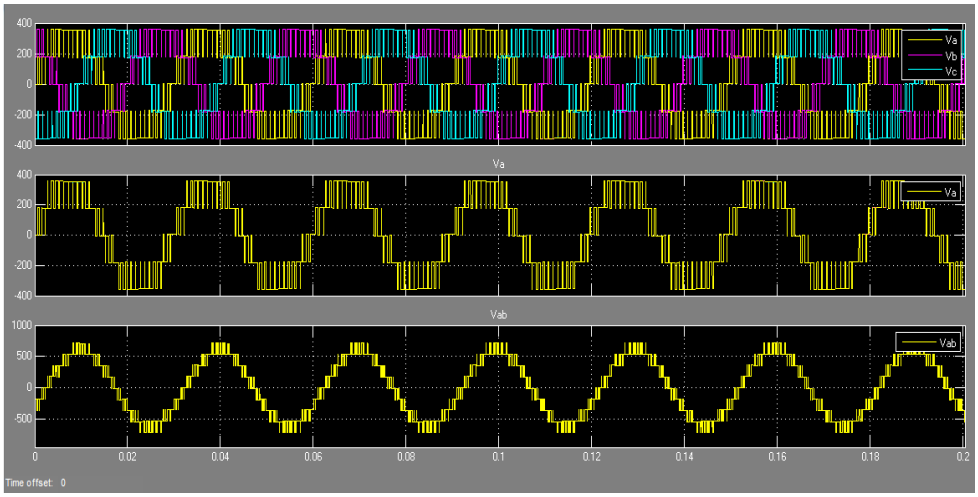

Fig. 12: Seven level MMCMLI output voltages

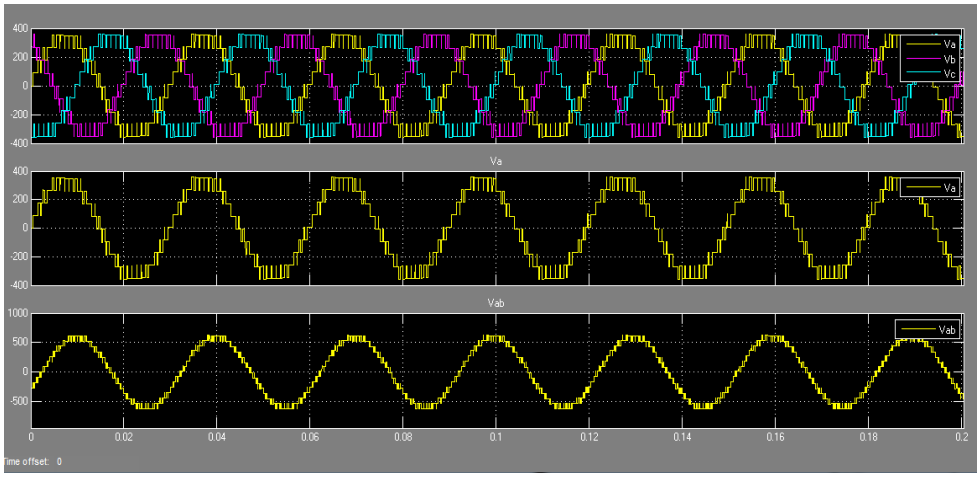

Fig. 13: Nine level MMCMLI output voltages

blocks 3, 4 and 6 operate as the controller for the system. The operating mode of the machine is controlled by the sign of the load torque. This is used to detect the machine operating mode and the switch on the breaker in block 3 if the machine is motoring or block 6 if the machine is generating. In practical implementation of this project, the operating mode of the machine can be determined by sensing the stator current direction. The block 5 consists of the permanent magnet synchronous machine which is used in traction application because of its high efficiency, more dynamic performance, smaller size and higher electrical stability. The universal rectifier which converts the ac power that is generated by the machine during regenerative braking to dc is shown in block 7. The integration of the MMCMLI system with PMSM is shown in Fig. 14. The operation of PMSM using three, five, seven and nine level inverters is shown in Fig. 17-20.

Table 3: Harmonic analysis of MMCMLI

		Total harmonic distortion (%)
Number of levels	Line-to-neutral	Line-to-line
Three		
Voltage	52.64	35.44
Current	9	
Five		
Voltage	27.26	17.28
Current	8.82	
Seven		
Voltage	18.66	10.82
Current	8.82	
Nine		
Voltage	13.72	8.53
Current	8.42	

Figure 17-20 shows the results of the simulation of the multi-module cascaded multilevel inverter that feeds the PMSM at a frequency of 33.4 Hz. The voltage outputs

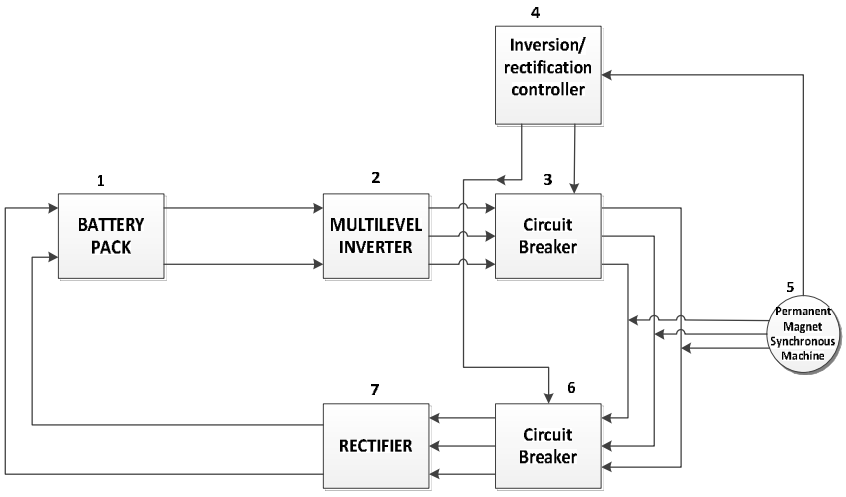

Fig. 14: General block diagram of the complete system

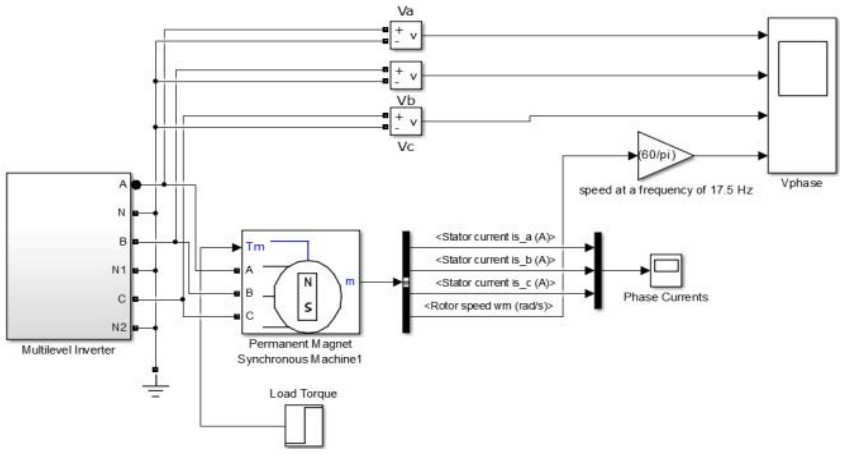

Fig. 15: Simulation model of MMCMLI with PMSM

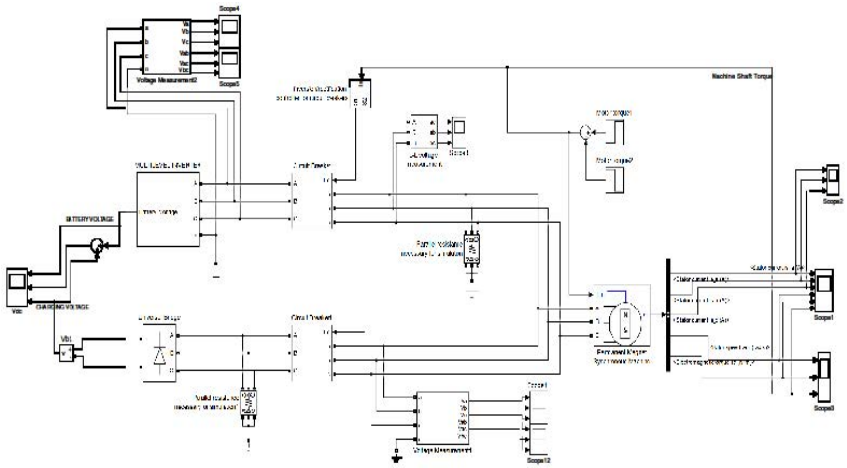

Fig. 16: Complete system with MMCMLI and PMSM

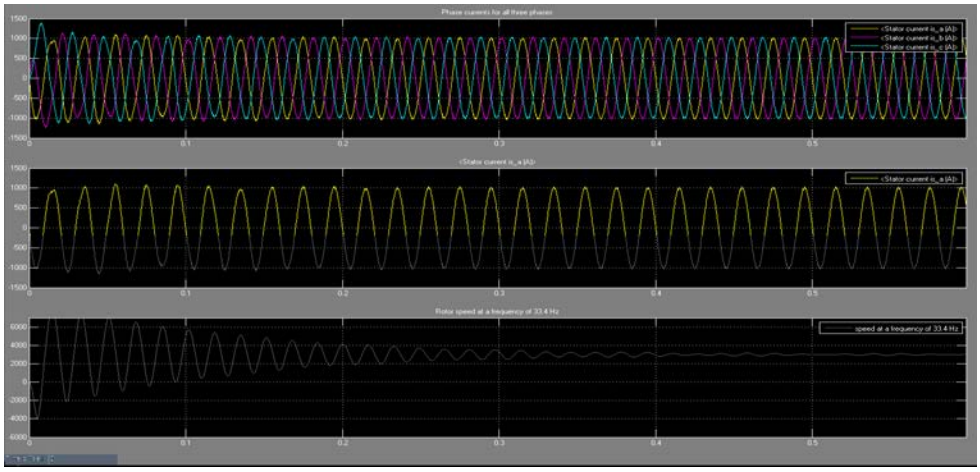

Fig. 17: Three level MMCMLI currents and speed at a frequency of 33.4 Hz

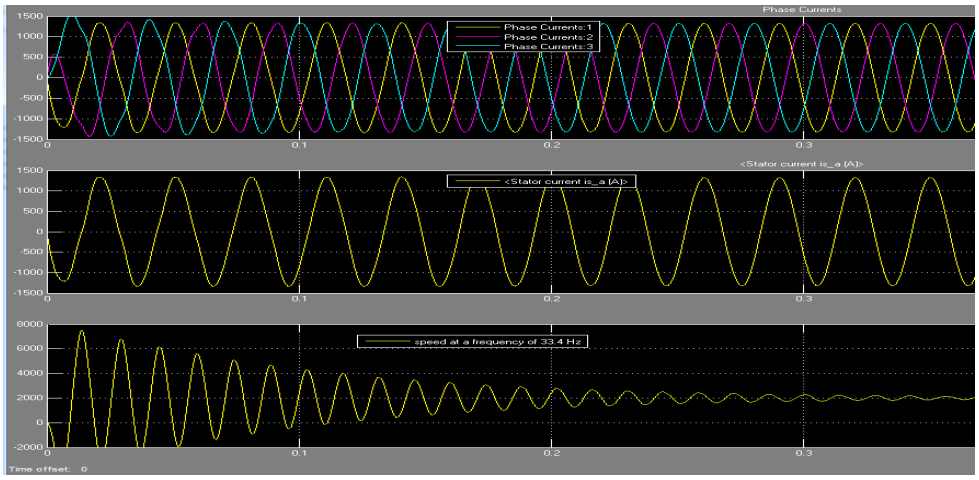

Fig. 18: Five level MMCMLI output currents and PMSM speed at a frequency of 33.4 Hz

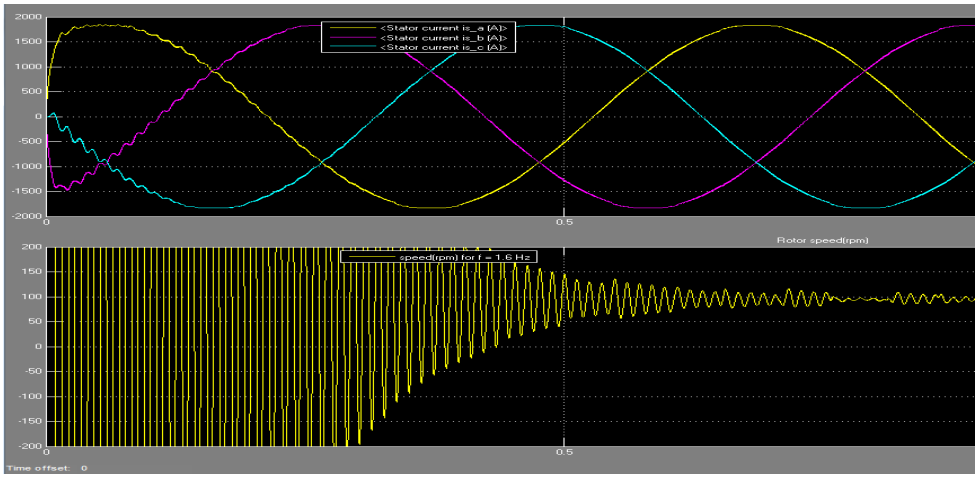

Fig. 19: Seven level MMCMLI output currents and PMSM speed at a frequency of 33.4 Hz

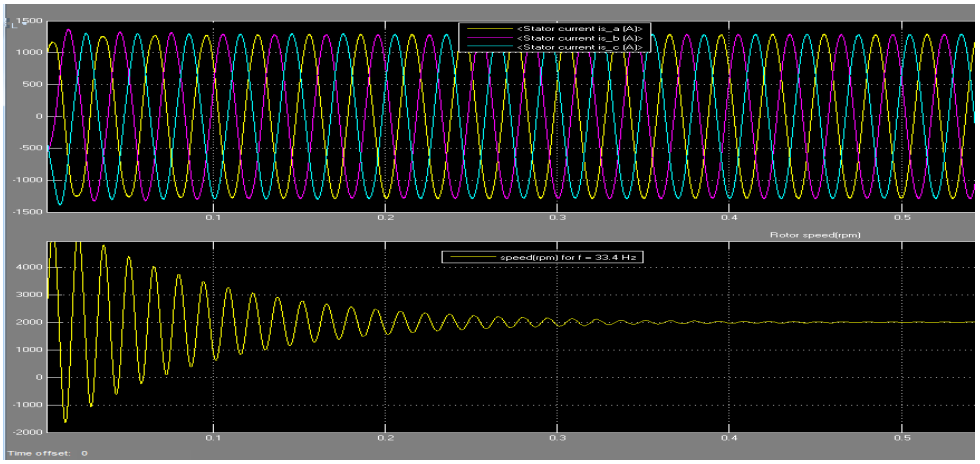

Fig. 20: Nine level MMCMLI output currents and PMSM speed at a frequency of 33.4 Hz

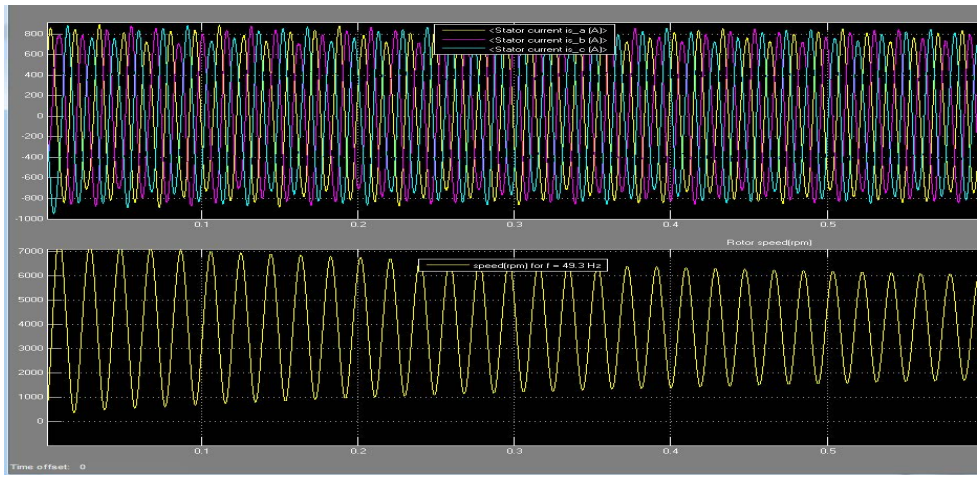

Fig. 21: Phase Currents and speed at f = 1.6 Hz

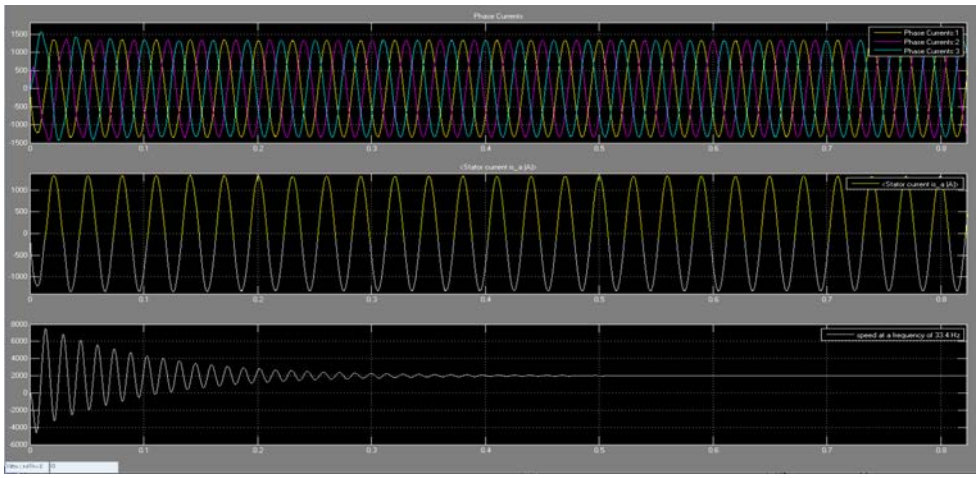

Fig. 22: Phase Currents and speed at f = 17.5 Hz

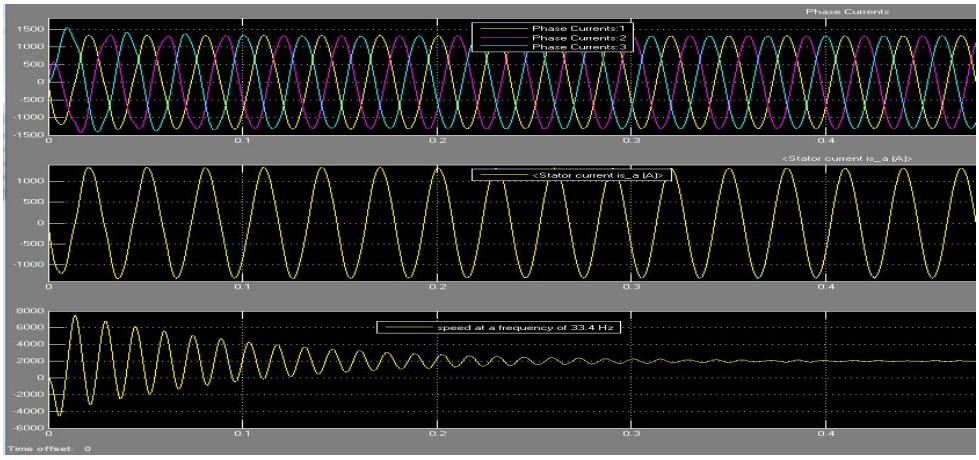

Fig. 23: Phase Currents and speed at f = 33.4 Hz

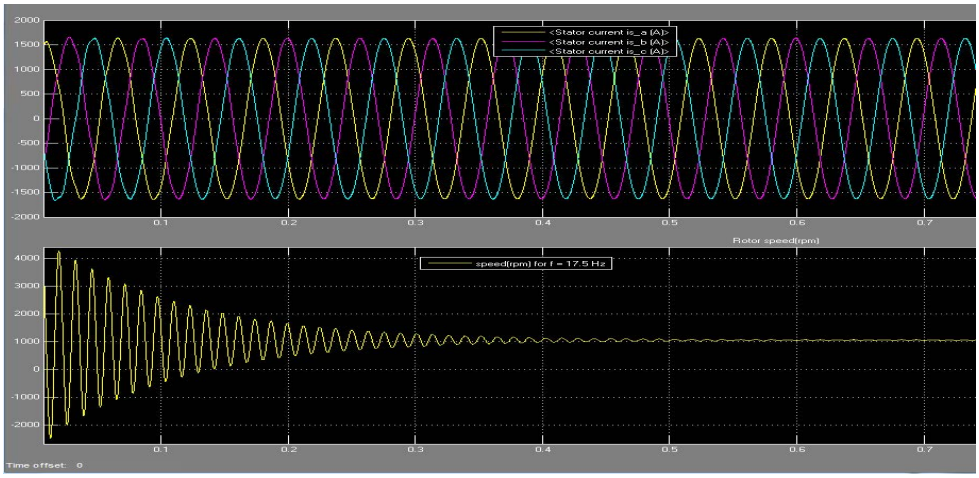

Fig. 24: Phase Currents and speed at f = 49.3 Hz

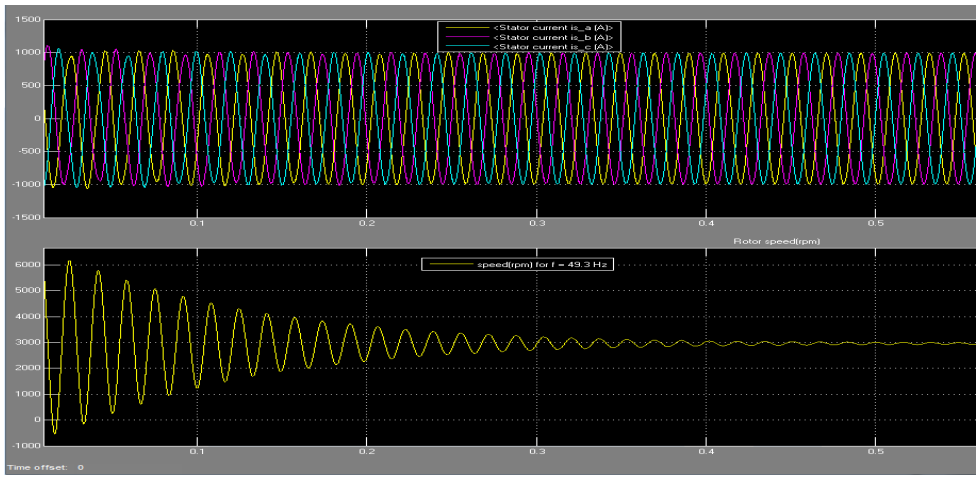

Fig. 25: Phase Currents and speed at f = 65.3 Hz

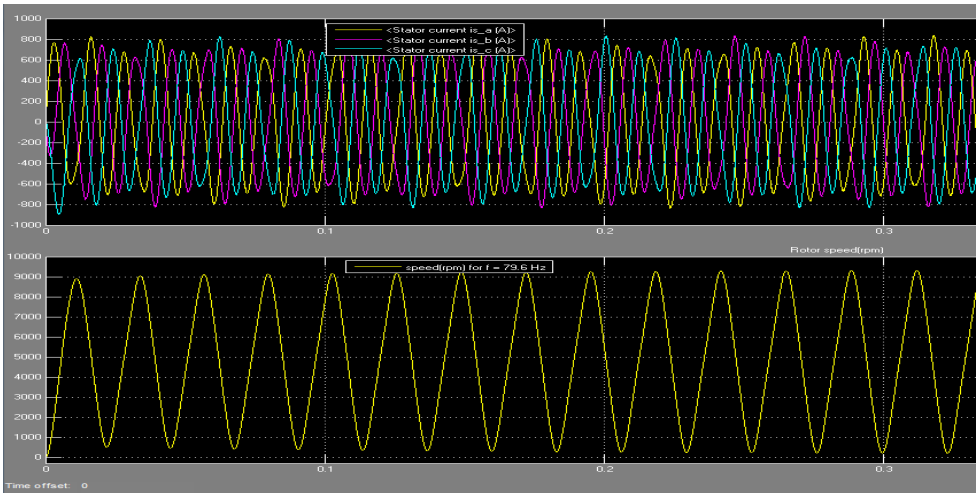

Fig. 26: Phase Currents and speed at f = 79.6 Hz

Table 4: PMSM speed variation

Frequency (Hz)	ω (rad/sec)	Rotor speed n(rpm)
1.6	10	95
17.5	110	1045
33.4	210	1995
49.3	310	2945
65.3	410	3895
79.6	500	4750

are observed to approach the sinusoidal waveforms of 33.4 Hz as the number of levels is increased from three to nine. Consequently, PMSM stator currents also conform to this trend, their THD decreases as the number of levels is increased. The THDs for the signals in Fig. 17-20 are shown in Table 3. This behavior is consistent with that discussed in the literature.

Furthermore, the machine speed shows a decrease in the magnitude of the initial oscillations as the number of levels is increased. However, the steady state value of the speed remains constant as long as the frequency is not changed.

The system shown in Fig. 16 is used to investigate speed variation of the PMSM. The frequency was varied as shown in Table 4 and the graphs in Fig. 21-26 were obtained.

CONCLUSION

In this research, solar powered multi-module cascaded multi-level inverter is designed to increase the efficiency of PMSM at different frequency operations. The incremental conductance algorithm is used to regulate the duty cycle of boost converter. The IC algorithm is preferred compared to P&O algorithm due to its stability at maximum power point. The MMCMLI is designed to get power the input power from either boost converter or battery. The efficiency of the motor depends on the efficiency of the inverter and its modulation techniques. Different types of multi-level inverter and their control strategies are discussed in the introduction section. It can be seen that the chosen phase in disposition modulation algorithm can effectively reduce the harmonics at 5, 7 and 9 level MMCMLI. The MMCMLI can also able to drive PMSM stably at different operating frequencies. This shows that the designed converter increases the efficiency and stabilizes the motor output at a frequency closer to the rated frequency. It can also be noted that the distortions in the phase current at low frequencies are very high. This shows that the chosen phase in disposition modulation technique is ineffective in operating the converter at low frequencies. This can be improved by implementing artificial intelligence techniques such as fuzzy and Artificial Neural Networks (ANN). The fuzzy logic method depends on the human training capability where as the ANN network can be trained for particular operation so that the algorithm can generate required modulation signals depending on the load characteristics. This will reduce the harmonics generated by the converter and increase the efficiency of PMSM in any speed control applications.

ACKNOWLEDGEMENTS

Wish to thank Mr. Rischave Pillay, Mr. Cinyama Mushid and Mr. Khanyasini Mlondo for their contribution to this research.

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