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A Novel Design of 7-Level Diode Clamped Inverter

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Abstract: A novel design of 7-level Diode Clamped Inverter (DCI) with one voltage source, 6 capacitors in series connected in parallel with the source, 12 diodes and 6 switches is presented with a new strategy using direct pulse generator with logic points to operating the proposed inverter are introduced. This study discusses the main features of 5 and 7-level DCI and some technical problems such as losses, cost and Total Harmonic Distortion (THD). Experimental results and simulations of the inverter with the control strategy are presented in MATLAB/Simulink to assure the efficiency of this logic control process.

Key words: 7-level DCI, pulse generator, THD, strategy, simulations, inverter

INTRODUCTION

Since, the previous century, a Multi-Level Inverter (MLI) was bounded to simple levels with time, growing applications, devices that be based on the MLI as an incoming type of power converters changed these simple circuits to a complex form with higher levels.

A MLI is widely used because it can eliminate the need for a step-up transformer and reduce O/p waveform harmonics especially when it greater than three levels. MLI divided into three topologies (common on voltage source) (Colak *et al*., 2011; Lega, 2007):

- Flying capacitors inverter. Using capacitors to carry a little amount of voltage to the switches
- Diode-clamped inverter. Using diodes to carry a little amount of voltage which leads to reducing the stress on switches
- Cascade H-bridge inverter. Using capacitors and switches with minimal components

Multi-level DCI who used in many implementations, especially at high power circuits because it has many concession at the essential frequency it supply the high qualification for switching.

The main advantage of using clamping dc bus voltage by using diodes it gives a limited value of voltage (achieving steps in O/p voltage), thereby, it minimizes the stress on other devices is the main concept from using diodes in DCI. Quality of O/p voltage gets better by increasing voltage levels number while the o/p waveform is nearer to sinusoidal.

Major benefits of DCI:

- Avoid needing filters when harmonics is minimum, this achieved by using high levels
- Efficiency is better due to all devices switched on essential frequency
- Simplicity in control strategy

Major DE benefits of DCI:

- Required a huge number of clamping diodes when levels number rise up
- Difficulty in control the real power inflow of the nonesuch converter

When these levels rise up extra than five level, be troublesome cause it needs more elements, leads to more losses, cost and complication in switching control and structure (Rodriguez *et al*., 2002; Lin and Chen, 2002; Holmes and McGrath, 2001; Bouhali *et al*., 2007), on the contrary THD be less when the level increase (Bowes and Holliday, 2006). Circuit components of the n-level DCI (Rashid, 2009; Mohan *et al*., 2003):

$$[(n-1)] \text{ Capacitors} \quad (1)$$

$$[(n-1)(n-2)] \text{ Diodes} \quad (2)$$

$$[2(n-1)] \text{ Switches} \quad (3)$$

Thereby, 3-level DCI configured from two capacitors, two diodes and four switches as in Fig. 1. The 5-level DCI configured from 4 capacitors, 12 diodes and 8 switches. The 7-level DCI configured from 6 capacitors, 30 diodes and 12 switches and so on.

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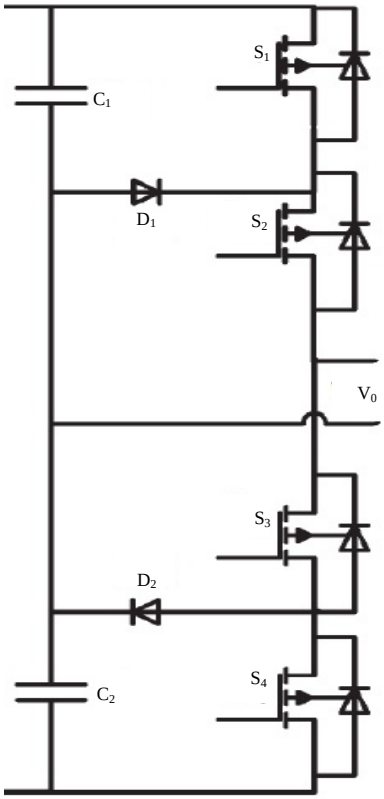

Fig. 1: The 3-level DCI

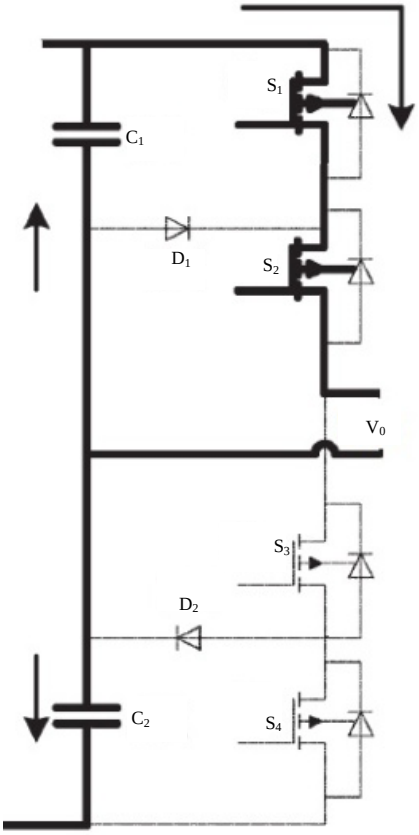

Fig. 2: Step 1 (t = t.-t.)

MATERIALS AND METHODS

Inverter operation (literature review)

The 3 level DCI using Pulse Width Modulation (PWM): DC voltage source rated as a fixed source, the voltage for each capacitor is same (V./2) the capacitors connected in series and in parallel with the voltage source. Thereby, the voltage on each switch is V./4.

Step 1 (t = t.-t) (Fig. 2): S. and S. are ON (for D/2f. period). Energy flows from the dc-link capacitor C. to O/p load. I/p currents rise and the voltage at O/p diode bridge is zero. The supply voltage is assumed to be constant within a switching cycle (due to high switching frequency). Where, f. is switching frequency and D is duty cycle.

Step 2 (t = t.-t) (Fig. 3): S. is OFF and S. remains ON. This step ends when current approximately reaches zero and lasts for .s, k/2f. amount of time:

$$\Delta s, k = \left(\left|Vk\right|D\right)/\left(V_{bus}-\left|Vk\right|\right) \quad (4)$$

.s, k = normalized period of step 2. This step time varying duration with one ac line-period. .s, k must satisfy [(.s, k+D)<1] for any load conditions and any interval k. To ensure a discontinuous I/p current:

$$V_{bus} > \left(\left|Vk\right|/\left(1-D\right)\right) \quad (5)$$

Step 3 (t = t.-t) (Fig. 4): Primary current circulates through D. and S., no energy transferred to O/p.

Step 4 (t.-t) (Fig. 5 and 6): S. and S. are OFF, through diodes body of S. and S. primary current charges C.. At the end of this step, S. and S. are switched ON (half switching cycle are finish). For the other half cycle, inverter goes for same steps 1-4, S. and S. are ON instead of S. and S..

Step 5 (t = t.-t): S. and S. are ON same period is beginning. The energy are flow from capacitor C. tothe O/p.

Step 6 (t = t.-t): S. is ON and S. is OFF. The energy stored from previous step absolutely transfer to the dc link apacitor.

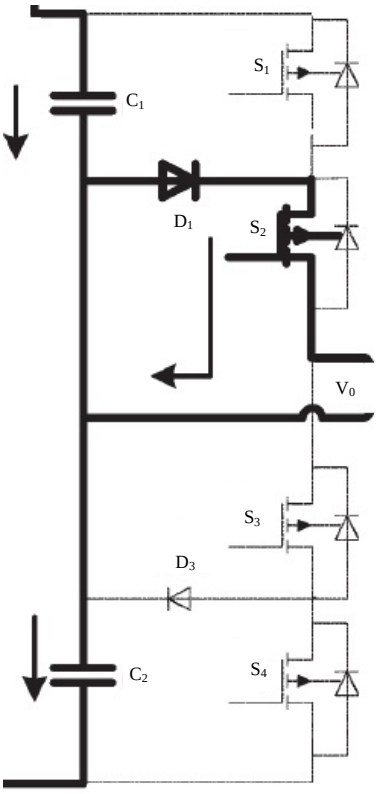

Fig. 3: Step 2 (t = t-t)

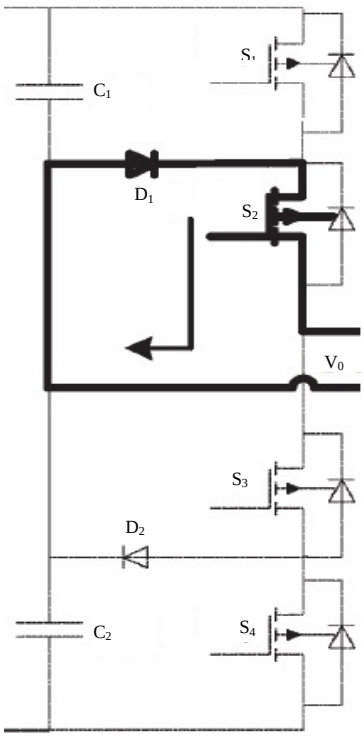

Fig. 4: Step 3 (t = t-t)

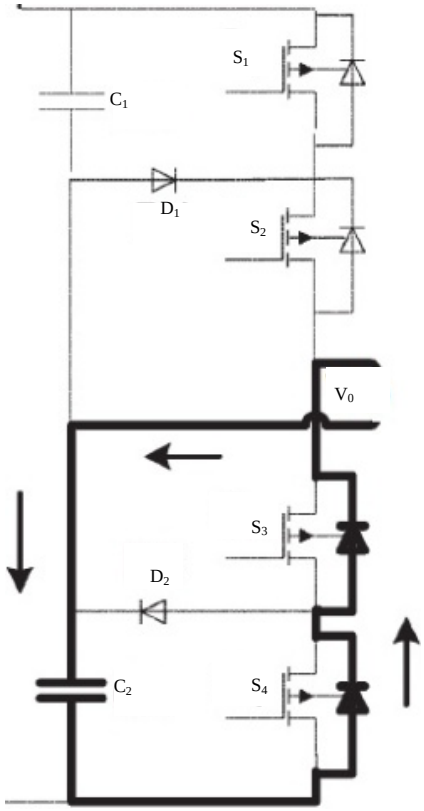

Fig. 5: Step 4 (t = t-t)

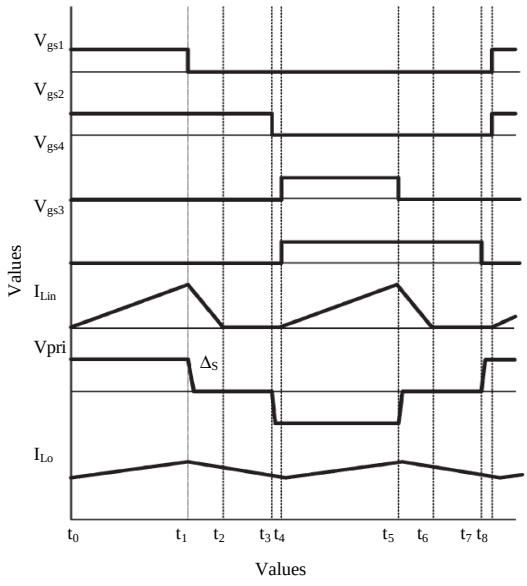

Fig. 6: Typical waveforms for modes of operation

Step 7 (t = t- t): S. OFF, the primary current circulates through the diode D. and S..

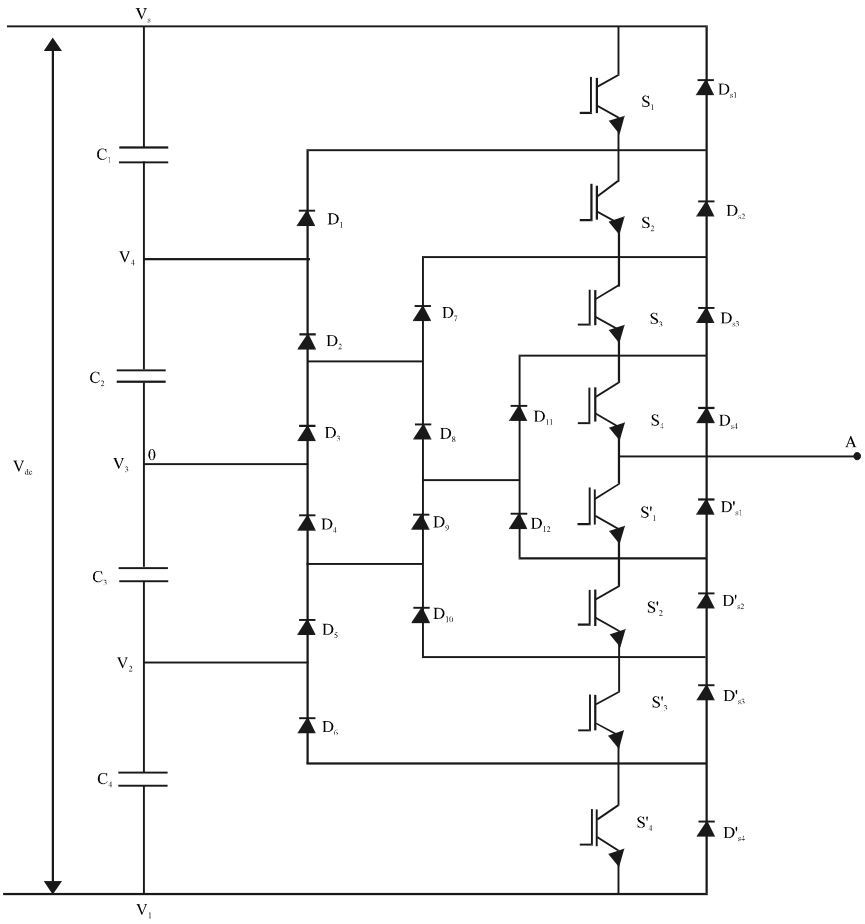

Fig. 7: The 5-level DCI

Step 8 (t = t-t): S. and S. are OFF, through diodes body of S. and S. primary current charges the capacitor C.. At end of this step, S. and S. are switched ON. O/p voltage regulation done by using a standard control methodology that controlling D. D is defined as the time during first half cycle (S. and S. are ON) or during the second half cycle (S. and S. are both ON). The inverter control implemented by using PWM technology (Patella *et al*., 2003; Zhang *et al*., 2013).

The 5 level DCI (using direct pulse generator): The voltage of each capacitor is same (V../4). Thereby, the voltage on each switch is V../4. The modes of switches VS magnitude of O/p voltage are listed in Table 1. The 4 switches for each mode (ON) and 4 switches (OFF) with different O/p (Gao *et al*., 2010; Loh *et al*., 2007a, b, 2008). DC bus voltage share into 5 levels by 4 capacitors C.-C. connected in series. A knowing as the neutral point as shown as in Fig. 7 and 8.

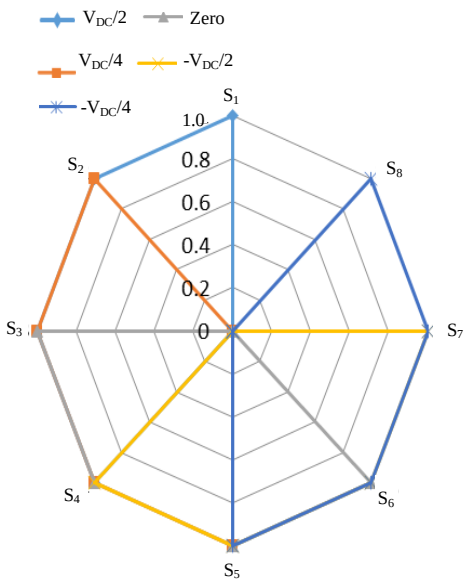

Fig. 8: Sector divisions of conventional 5-level

Table 1: The 5-level DCI switching sequence vs. O/p voltage magnitude

O/P voltage	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
$V_{DC}/2$	ON	ON	ON	ON	OFF	OFF	OFF	OFF
$V_{DC}/4$	OFF	ON	ON	ON	ON	OFF	OFF	OFF
Zero	OFF	OFF	ON	ON	ON	ON	OFF	OFF
$-V_{DC}/2$	OFF	OFF	OFF	ON	ON	ON	ON	OFF
$-V_{DC}/4$	OFF	OFF	OFF	OFF	ON	ON	ON	ON

RESULTS AND DISCUSSION

Proposed 7-level diode clamped inverter: Depending on the rules (1:3), 7-level DCI configured from six capacitors, 30 diodes and 12 switches!. Proposed 7-level DCI with 6 capacitors, 12 diodes and 8 switches as in Fig. 9. By

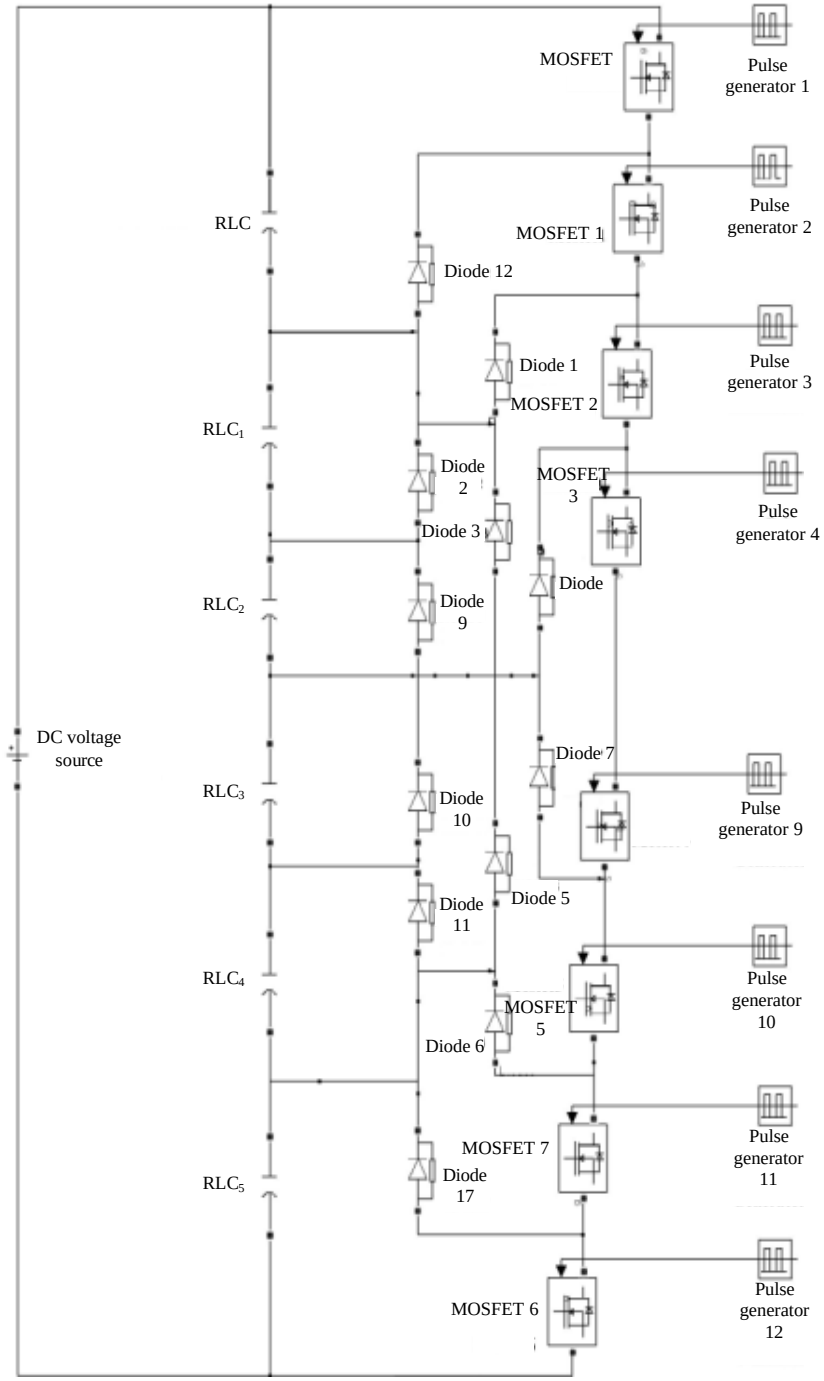

Fig. 9: Proposed 7-level DCI

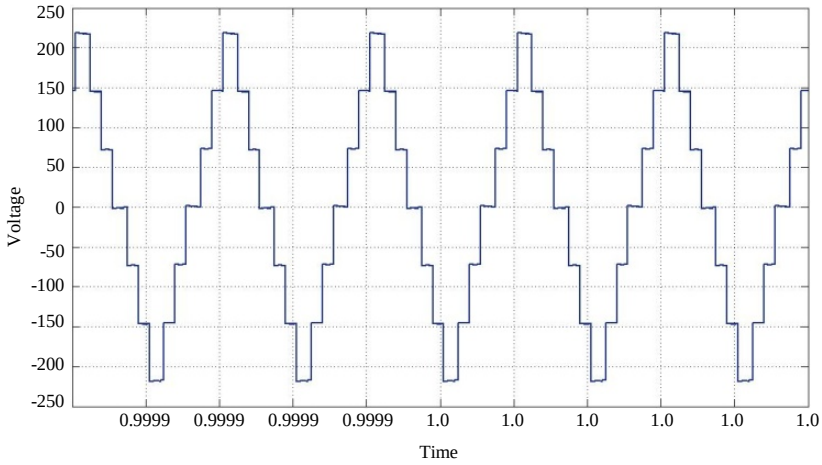

Fig. 10: The 7-level DCI O/p voltage

cancellation 18 diodes and 4 switches, compensation by new control strategy. Proposed inverter gives same levels with fewer elements, cost and complexity.

Switching scheme is to warranty that switches action in tangent style. O/p voltage Van has seven cases (V$_{dc}$/2), (V$_{dc}$/4), (V$_{dc}$/8), (0), (-V$_{dc}$/8), (-V$_{dc}$/4), (-V$_{dc}$/8) as shown in Fig. 10. These 7 cases achieved when depending on the newer logic states:

- Upper switches (S$_1$-S$_2$) be ON and all lower switches (S$_3$-S$_4$) be OFF to get (V$_{dc}$/2)
- Switches (S$_1$-S$_2$) be ON, S$_3$ and all lower switches (S$_4$-S$_6$) be OFF to get (V$_{dc}$/4)
- Switches (S$_1$ and S$_2$) be ON, S$_3$, S$_5$ and all lower switches (S$_4$-S$_6$) be OFF to get (V$_{dc}$/8)
- Switches (S$_1$ and S$_2$) be ON (S$_3$-S$_6$) be OFF to get (zero)
- Switches (S$_1$ and S$_2$) be ON, S$_3$, S$_5$ and all upper switches (S$_3$-S$_4$) be OFF to get (-V$_{dc}$/2)
- Switches (S$_3$-S$_4$) be ON, S$_1$ and all upper switches (S$_1$-S$_2$) be OFF to get (-V$_{dc}$/4)
- Lower switches (S$_4$-S$_6$) be ON and all upper switches (S$_1$-S$_3$) be OFF to get (-V$_{dc}$/8) (Table 2). Using direct pulse generator

Control strategies In MATLAB program by using the parameters in source block of each switch (amplitude, period, pulse width and phase delay) by issuing a square wave at fixed intervals are called pulse generator. Amplitudes are one for all switches with period 1/f, phase delay and pulse width are changing depending on Table 2. As an example switch, 1 is one time ON in V$_{dc}$/2 O/p and OFF for all other time, works of 10% from life cycle.

Table 2: Proposed 7 level DCI switching sequence vs. O/p voltage

O/P voltage	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
$V_{DC}/2$	ON	ON	ON	ON	OFF	OFF	OFF	OFF
$V_{DC}/4$	OFF	ON	ON	ON	OFF	OFF	OFF	OFF
$V_{DC}/8$	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF
Zero	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF
$-V_{DC}/2$	OFF	OFF	OFF	OFF	ON	ON	OFF	OFF
$-V_{DC}/4$	OFF	OFF	OFF	OFF	ON	ON	ON	OFF
$-V_{DC}/8$	OFF	OFF	OFF	OFF	ON	ON	ON	ON
$-V_{DC}/4$	OFF	OFF	OFF	OFF	ON	ON	ON	OFF
$-V_{DC}/2$	OFF	OFF	OFF	OFF	ON	ON	OFF	OFF
Zero	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF

Switch 1 works without delay, so phase delay equal to zero and pulse width equal to 12.5% of the period. Switch 2 works without delay, so, phase delay equal to zero also. Switch 2 is two time ON in V$_{dc}$/2 and V$_{dc}$/4, OFF for all other time, so, pulse width equal to 25% of the period and so on for other switches as Fig. 11. This inverter prepared according to the next specifications:

- I/p Voltage V$_{in}$ = 440 V
- Capacitors 100 μ Farad
- Switching frequency f$_{in}$ = 50 kHz
- O/p voltage 440 V pk-pk
- V$_{in}$ = V$_{in1}$+V$_{in2}$+V$_{in3}$+V$_{in4}$+V$_{in5}$+V$_{in6}$
- V$_{in1}$ = V$_{in2}$ = V$_{in3}$ = V$_{in4}$ = V$_{in5}$ = V$_{in6}$ = V$_{dc}$/4
- Period time = 1/f$_{in}$.

One of the main advantages of this design is the THD, classical 7 level DCI which configured from 6 capacitors, 30 diodes and 12 switches had about 23.52 % THD while proposed inverter has only 21.89% as in Fig. 12 and 13.

Comparing classic and proposed topology for 7 level DCI are shown in Table 3. Both of them have same levels but newer one configured with fewer diodes and switching devices, the most important advantages are THD.

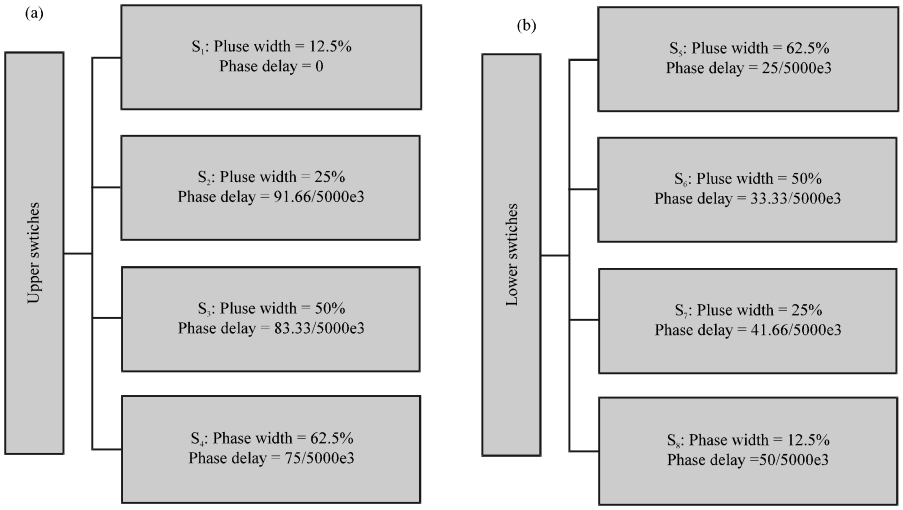

Fig. 11: Pulse width and Phase delay for upper and lower switches

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Sampling time     = 5e-07 s
Samples per cycle = 40
DC component      = 7.969e-08
Fundamental       = 40.88 peak (28.91 rms)

Total Harmonic Distortion (THD) = 23.52%

Maximum harmonic frequency
 used for THD calculation  = 950000.00 Hz (19th harmonic)

     0 Hz  (DC):          0.00    270.0°
```

Fig. 12: Conventional 7-level DCI THD

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Sampling time     = 5e-07 s
Samples per cycle = 40
DC component      = 0.7707
Fundamental       = 46.37 peak (32.79 rms)

Total Harmonic Distortion (THD) = 21.89%

Maximum harmonic frequency
 used for THD calculation  = 950000.00 Hz (19th harmonic)

     0 Hz  (DC):          0.77     90.0°
```

Fig. 13: Proposed 7-level DCI THD

Table 3: Classic and proposed topology comparison

Topology	No. of capacitors	No. of diodes	No. of switches	THD (%)
Classic topology	6	30	12	23.520
Proposed topology	6	12	8	21.890

CONCLUSION

Inverter levels growing, amount of semiconductors are growing also, this leads to increase losses, cost, control complexity (especially more than 5 level). Changing control strategy offer to us a new design of 7-level DCI (configured only from 6 capacitors, 12 diodes and 8 switches. Proposed 7-level DCI resolve almost all the prior problems, it produces the same level number with fewer elements and less THD (21.89%). A new design of 7-level DCI using fewer elements, smaller size and installation cost with maximum efficiency.

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